TECHNICAL MANUAL

FOR THE

R-110 RECEIVER

This manual is intended for use with

the following serial number:

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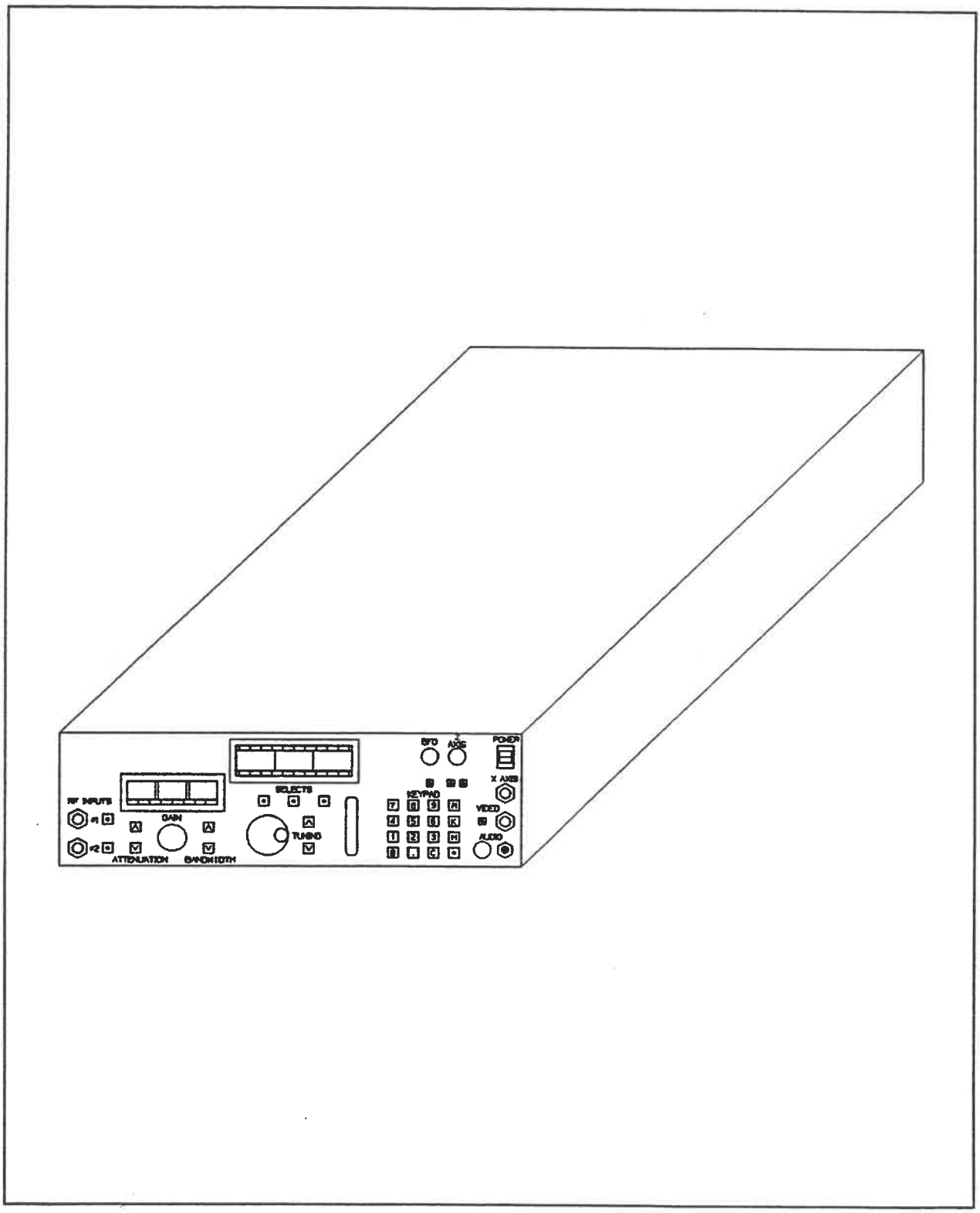

Frontispiece

INTRODUCTION

This manual provides operation, installation, and maintenance instructions for the Dynamic Sciences R-110 receiver. The purpose of the receiver is to detect and demodulate RF signals over a frequency range of 1 kHz to 1 GHz. The receiver is designed for both laboratory and field operations.

The manual is organized in sections providing the following information:

Section 1, **Description of Equipment**, provides an overview of the receiver with listings of specifications, characteristics, equipment supplied, and additional equipment needed for installation and service.

Section 2, **Installation**, supplies the information required to unpack and install the equipment, including a listing of the physical characteristics of crated equipment, cable requirements, installation procedures, and preparations required for reshipment.

Section 3, **Operating Instructions**, provides a discussion of the controls and indicators, along with detailed operating instructions. Information regarding instrument initialization and fault indications are included in this section.

Section 4, **Theory of Operation**, includes an overview discussion of system operation and in-depth detailed discussions of the functional operation of the electronic circuits and mechanical assemblies. The explanation of circuit functions are supported by signal flow diagrams for each of the major sections.

Section 5, **Maintenance**, provides information for maintaining and repairing the receiver. Beginning with a listing of recommended periodic maintenance, the section includes a detailed performance test designed to demonstrate that all of the receiver functions are operating properly, to a high degree of confidence. Following the maintenance procedures, further procedures are given for fault isolation, mechanical disassembly of the radio, and field service adjustments for newly installed modules.

Section 6, **Parts Lists and Circuit Diagrams**, includes parts lists for all sections of the receiver, with reference designations and a listing of manufacturers. This chapter also provides circuit diagrams for all sections of the receiver, including reference designaltions tied to the associated parts lists.

Appendix A, **IEEE-488 Interface Protocol**, lists the compatibility level supported for each standard IEEE-488 function, lists and describes the supported IEEE-488.2 standard protocols and commands, and lists and describes the additional interface protocols and commands unique to the R-110.

Appendix B, **Hardware Address Map**, gives the port addresses of all of the hardware which communicates with the controlling microprocessor. Usage of individual bits in these ports, and usage of read vs. write ports at the same address, are given where necessary.

SECTION 1. DESCRIPTION OF EQUIPMENT

1.1 Description and Purpose

The R-110 receiver, shown in the frontispiece, is a solid-state multiple-conversion receiver that provides a means of detecting and measuring signals associated with electromagnetic analysis, TEMPEST, spectrum analysis, and frequency surveillance, in the range of 1 kHz to 1 GHz. Three basic modes of operation are incorporated into the instrument: manual operation, automated sweeping, and remote operation controlled by a host computer. The receiver will also work with various accessories such as the R-1180 microwave downconverter, which extends the frequency range to 18 GHz.

1.2 Equipment Description

The R-110 receiver consists of modularly-constructed electronic circuits integrated with a front panel assembly containing operator controls and indicators. RF, video, and analog signals are interconnected by dedicated connectors located on the front and rear panels of the instrument. Function control signals and interface data used by separately mounted equipment are provided through multi-contact connectors that use distinctive configurations to prevent improper positioning when mated.

1.3 Physical Characteristics

The physical characteristics of the R-110 are shown in table 1-1.

1.4 Specifications

The detailed electrical and performance specifications of the R-110 receiver are shown in table 1-2. Each entry is prefaced with the applicable paragraph number from section 4.3.3 of the SOW or a "DSI", indicating that the item is in addition to the specified requirements. An "*" indicates that the specification paragraph has been revised. The "As Designed" entries show the anticipated operation/performance of the prototype and production receivers; a "Same" means "same as specified requirement". The "Specification" entries are from the SOW and approved revisions.

Table 1-1: Physical Characteristics

Line Voltage	115/230 VAC ± 10%
Power Dissipation	100 Watts
Mechanical Dimensions	
Standard Height	5.22" (133 mm)
Standard Width	17.00" (432 mm)
Standard Depth	20.50" (521 mm) (plus depth of front panel controls)
Rack Mount Height	5.22" (133 mm)
Rack Mount Width	19.00" (483 mm)
Rack Mount Depth	20.50" (521 mm) (plus depth of front panel controls)
Weight	39 lbs (18 kg)
Volume	1.0 cu ft
Cooling	Free/forced convection
Temperature Range	
Operating	+40° - +105° F (+5° to +40° C)
Storage	-40° - +167° F (-40° - +75° C)
Relative Humidity	
Operating	0 - 90% non-condensing
Storage	0 - 95% non-condensing

Table 1-2: Specifications

Feature	Specification
Modes of Operation	Manual, scan, and remote (standard); downconverter (optional)
RF Inputs	Two inputs, remotely or locally selectable, break-before-make switching
Frequency Range	Both inputs tunable from 1 kHz to 1 GHz
Noise Figure	10 dB (10)
Spurious-Free Dynamic Range	Not less than 60 dB between RF input and AM video output, and between RF input and IF output
RF Input VSWR	Less than 2:1 over full frequency range
RF Input Impedance	50 Ohms nominal
Maximum Tolerated RF Input	1 Watt average CW
Isolation Between RF Inputs	At least 80 dB
LO Leakage at RF Inputs	Less than -90 dBm
Residual Spurious Responses	Less than -107 dBm
IF Rejection	At least 80 dB
Image Rejection	At least 80 dB
RF Input Attenuator: Range Operation Switching Time	 0 - 70 dB in 10 dB steps Manual and autorange Less than 30 ms
Gain	Quasi-continuous, 50 dB range; RF, IF, predetection gains optimized

Table 1-2 Continued

Feature	Specification
Tuning Bands	Three bands, automatically selected
Band Switching Settling Time	30 ms typical
Band Frequency Ranges	1 kHz - 249.9999 kHz 250 kHz - 14.999999 MHz 15 MHz - 1 GHz (hysteresis provided across band breaks)
Tuning	Single knob tuning with selectable tuning rate; dual switches for pushbutton tuning; switches for automatic scan
Tuning Interference	No detectable tuning interference in video and audio outputs
Reference Oscillator Type	100 MHz oven-controlled quartz oscillator; trimmable
Reference Oscillator Aging	1 PPM per year
Reference Oscillator Temperature Stability	0.05 PPM, 0 - 60 °C
Reference Oscillator Output	Greater than 0 dBm
Receiver Frequency Stability	Same as reference oscillator after 30 minutes
Receiver Frequency Accuracy	Same as reference oscillator after 30 minutes
Frequency Display	12 digit alphanumeric LED, adjustable intensity
Frequency Display Readability	Visible in high or low ambient light

Table 1-2 Continued

Feature	Specification
Wideband IF Output Frequency	1450 MHz nominal
Wideband IF Output Level	At least -30 dBm into 50 Ohms
Signal Monitor Center Frequency	21.4 MHz
Signal Monitor Bandwidth	4 MHz minimum
Signal Monitor Output Level	At least -70 dBm with RF input of -107 dBm and full RF gain
IF Center Frequency	21.4 MHz
IF Bandwidths	500 Hz - 20 kHz in 1 - 2 - 5 sequence, 80 kHz, 300 kHz, 1 MHz, 4 MHz, 15 MHz (standard set); 200 Hz - 20 kHz in 1.0 - 1.25 - 1.6 - 2.0 - 2.5 - 3.2 - 4.0 - 5.0 - 6.4 - 8.0 sequence, 80 kHz, 300 kHz, 1 MHz, 4 MHz, 15 MHz (extended set)
IF Impulse Response	Overshoot less than 8% for bandwidth less than 150 kHz, less than 12% for bandwidth greater than 150 kHz
IF Selectivity	Shape factor better than 4:1 (60 to 6 dB) typical
IF Output Level	At least 10 dBm into 50 Ohms
AGC	Selectable with keypad
Detection Modes	AM, CW
Detection Type	AM peak

Table 1-2 Continued

Feature	Specification
Video Outputs	AM linear or log, Z axis
Optional Video Functions	Slideback, pulse stretch
Video Bandwidth	Not less than 1/2 selected IF bandwidth
Linear Video Dynamic Range	At least 30 dB
Log Video Dynamic Range	At least 60 dB
Video and Z Axis Output Impedance	50 Ohms nominal
Video Output Level	At least 4 Volts into 50 Ohms
Z Axis Controls	Output adjustable to 3 Volts RMS and invertible
Audio 3 dB Frequency Response	20 Hz - 20 kHz
Audio Output Level	At least 2 Volts RMS into 8 Ohms
BFO Tuning Range	At least 4 kHz
BFO Tuning Resolution	Continuous
IEEE-488 Capability Levels	SH1, AH1, T6, L4, SR1, RL1, PP0, DC1, DT0, C0
IEEE-488 Controllable Functions	Input selection, input attenuation, bandwidth, gain, tuned frequency, video selection, AGC, and others
Power Cord	Shielded cord
Protection From AC Line Voltage	No damage when improper voltage applied
Line Voltage Range Selection	Rotary switch

1.5 Equipment Supplied

The equipment and accessories supplied are shown in table 1-3.

Table 1-3: Equipment Supplied

QTY	DSI PART NUMBER	DESCRIPTION
1	493000	R-110 FTTR Receiver
1	493000OM	Operator's Manual
1	493012	Cable W1, AC Power

1.6 Equipment Required But Not Supplied

Certain equipment is required for installation or service of the receiver, but must be supplied by the user. Table 1-4 lists these items.

Table 1-4: Equipment Required But Not Supplied

QTY	DESCRIPTION
1	Ground Strap

1.7 Optional Equipment

Certain equipment is available from Dynamic Sciences, Inc., for use with the R-110 receiver which is not included in the basic package. Table 1-5 lists these items.

Table 1-5: Optional Equipment

Part No.	Description
493010	Service Kit
R-1180	Microwave Downconverter
R-1260i	Automated System Controller

SECTION 2. INSTALLATION

2.1 Introduction

This section provides installation information for the R-110 Receiver and includes interconnection data for integrating the receiver with associated equipment. Instructions for repacking the equipment for shipment are also provided.

2.2 Installation Planning

The R-110 Receiver is compact and portable, and can be used in various laboratory and field applications. All that is required is for operation is adequate power and ventilation. If the receiver is to be rack-mounted then the recommendation given for clearance within the rack for the purpose of ventilation should be followed.

2.3 Crating Data

The R-110 is packed in a specially constructed shipping container, as shown in figure 2-1, that protects the instrument during transit. Crate dimensions and weight are shown in table 2-1.

Table 2-1: Crating Data

Height	8 ⅜ in. (213 mm)
Width	22 ½ in. (572 mm)
Depth	27 ⅞ in. (708 mm)
Weight	50 lbs. (22.7 kg)

Note that the factory shipment includes an accessory package, separate from the crate containing the receiver, for the operator's manual and any other documentation.

2.4 Receiving Inspection

Each instrument is carefully tested and inspected prior to shipment. When unpacking, inspect the container and the instrument for evidence of shipping damage. If damage is indicated then notify the freight carrier immediately. Check each item against the packing list or the purchase order, to ensure that all items have been received. Determine that all instrument serial numbers are identical to the numbers shown on the packing list. If portions of the shipment are missing, and are not listed as back ordered items, then contact the freight carrier or Dynamic Sciences.

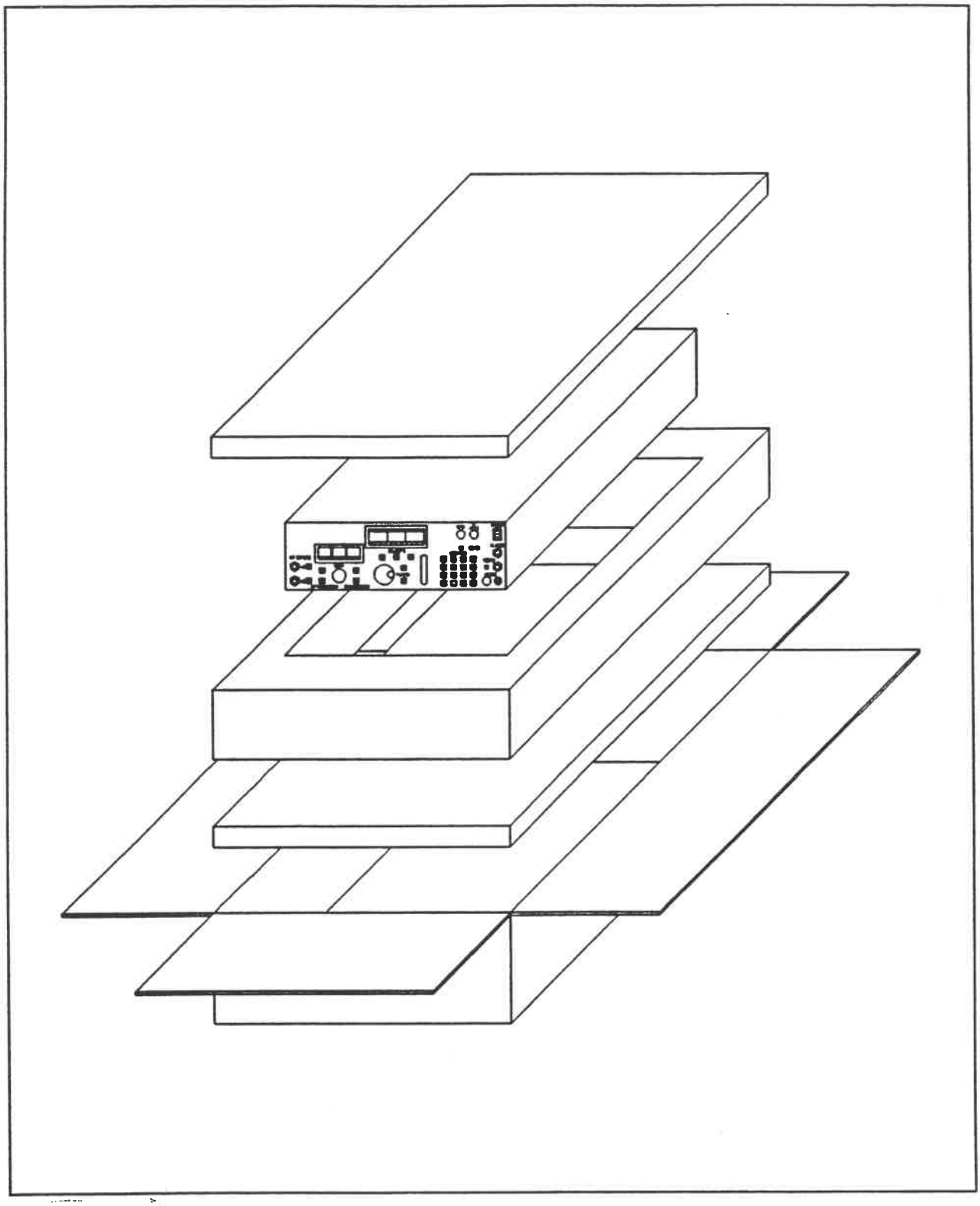

Figure 2-1: Equipment Packaging

2.5 Unpacking

Retain the shipping container and all packing material for subsequent shipments of the instrument, or when storage is required. When an instrument is returned to the factory for repair or modification, attach a tag to the instrument indicating service required, serial number, model number, and the complete return address.

Figure 2-1 shows the shipping container and contents.

Unpacking Procedure:

1. Slit the plastic tape around the top of the shipping container.
2. Open the top of the container.
3. Remove the top layer of shock absorbent material.
4. Remove the instrument from the shipping container by lifting straight up.
5. Ensure that accessory packages have been removed.

2.6 Mounting

The R-110 is designed for either bench operation or rack mounting. For bench operation insure that air-flow at the rear and sides of the instrument is not obstructed. When the instrument is rack mounted, a standard 19" RETMA rack with at least 20" depth is suitable. A minimum clearance of 1.0 inches at the rear of the instrument is required to ensure adequate free air movement. For rack mounting the optional slide rails are to be attached to the receiver's sides. When used in a system configuration, the location of the receiver and any associated components is not specified, and should be determined by the user.

2.7 Cable Requirements

Table 2-2 lists the cables required for operation of the receiver. The table indicates which cables are supplied.

Table 2-2: Connecting Cables

QTY	DSI PART NO.	DESCRIPTION	SUPPLIED
1	493012	W1, AC Power, 117 VAC	Yes
1	NA	W2, AC Power, 220 VAC	No
1	NA	W3, GPIB	No
1	NA	W4, Status	No

2.8 Equipment Connection

All signals interface with the receiver through connectors that are located on the front and rear panels of the instrument. Table 2-3 identifies the receiver's connectors.

Table 2-3: Connector Identification

Front Panel	
Function	**Type**
RF Input #1	Female BNC
RF Input #2	Female BNC
X Axis Output	Female BNC
Video Output	Female BNC
Audio Output	1/4" Phone Jack
Rear Panel	
Function	**Type**
Z Axis Output	Female BNC
Reference Oscillator Output	Female BNC
21.4 MHz IF Output	Female BNC
Signal Monitor Output	Female BNC
IEEE-488 Interface	Female 24 Pin D
Status/Control Output	Female 25 Pin D-Sub
AC Line Input	Male 3 Pin NEMA

2.9 Power Connections and Settings

The instrument is shipped from the factory preset to operate from a power source of 115 volts, 50/60 Hz, single phase. For operation using a different voltage range, select the proper fuse rating from table 2-4, and proceed as follows:

AC Range Selection Procedure:

1. Place the AC line voltage select switch located on the rear panel of the instrument in the proper position.
2. Select and install the proper line fuses for the AC line input voltage to be used.
3. Set the AC line voltage subrange switch to the required position as shown in table 2-5. When both the AC HI and AC LO indicators on the front panel are both extinguished, the range selected is acceptable.

Table 2-4: Fuse Selection

VOLTAGE	FUSE RATING
115 V Range	2 Amp, 2ASB slo-blo, Littelfuse 213002
230 V Range	1 Amp, 1ASB slo-blo, Littelfuse 213001

Table 2-5: Line Voltage Range Selection

SELECT SWITCH	SUBRANGE SWITCH	INPUT VOLTAGE RANGE
115 V	Low	95 - 105 VAC
	Norm	105 - 115 VAC
	High	115 - 126 VAC
230 V	Low	190 - 210 VAC
	Norm	210 - 231 VAC
	High	231 - 253 VAC

The instrument has a 3 conductor power cord which, when connected to an appropriate receptacle, grounds the instrument chassis for safety.

WARNING
THE AC POWER CORD SHOULD ONLY BE CONNECTED TO RECEPTACLES THAT HAVE ACTIVE PROTECTED EARTH GROUND CONTACTS. BYPASSING OR DEFEATING THE EARTH GROUND PROTECTION CAN RESULT IN INJURY TO OPERATING PERSONNEL.

2.10 External Interfaces

Pin numbers and signal identification for the IEEE-488 interface connector are listed in table 2-6.

The signal identification for the internally mounted RS-232 service connection is listed in table 2-8.

The R-110 comes factory-set to IEEE-488 interface address 16, and with the RS-232 interface set to a baud rate of 1200. To change either of them, perform the appropriate procedure, as follows:

IEEE-488 Address Setting Procedure:

1. Unplug the receiver. Remove the retaining screws from the cover and slide off of the chassis.

2. There is one dipswitch visible through the hatch on the underside of the front panel assembly. Switches 1 - 5 determine the bus address. The desired address must be set in binary, with switch 5 considered to be the MSB. "On" generates a zero, "Off" a one. Table 2-7 lists the setting for each available address.

3. When the dipswitch is set to the desired value, replace the cover and reassemble the receiver. The new setting will be read on power-up.

4. The bus address may be temporarily changed by means of the front panel controls, but this setting is lost when power is removed. See chapter 3 for details.

RS-232 Baud Rate Setting Procedure:

1. Unplug the receiver. Remove the retaining screws from the cover and slide off of the chassis.

2. There is one dipswitch visible through the hatch on the underside of the front panel assembly. Switches 6 - 8 determine the baud rate. The desired address must be set in binary, with switch 8 considered to be the MSB. "On" generates a zero, "Off" a one. Table 2-9 lists the setting for each available baud rate.

3. When the dipswitch is set to the desired value, replace the cover and reassemble the receiver. The new setting will be read on power-up.

Table 2-6: IEEE-488 Interface Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	DAV GND
7	NRFD	19	NRFD GND
8	NDAC	20	NDAC GND
9	IFC	21	IFC GND
10	SRQ	22	SRQ GND
11	ATN	23	ATN GND
12	SHIELD	24	LOGIC GND

Table 2-7: Dipswitch Settings for IEEE-488 Interface Address

ADDRESS	SWITCH				
	1	2	3	4	5
0	On	On	On	On	On
1	Off	On	On	On	On
2	On	Off	On	On	On
3	Off	Off	On	On	On
4	On	On	Off	On	On
5	Off	On	Off	On	On
6	On	Off	Off	On	On
7	Off	Off	Off	On	On
8	On	On	On	Off	On
9	Off	On	On	Off	On
10	On	Off	On	Off	On
11	Off	Off	On	Off	On
12	On	On	Off	Off	On
13	Off	On	Off	Off	On
14	On	Off	Off	Off	On
15	Off	Off	Off	Off	On
16	On	On	On	On	Off
17	Off	On	On	On	Off
18	On	Off	On	On	Off
19	Off	Off	On	On	Off
20	On	On	Off	On	Off
21	Off	On	Off	On	Off
22	On	Off	Off	On	Off
23	Off	Off	Off	On	Off
24	On	On	On	Off	Off
25	Off	On	On	Off	Off
26	On	Off	On	Off	Off
27	Off	Off	On	Off	Off
28	On	On	Off	Off	Off
29	Off	On	Off	Off	Off
30	On	Off	Off	Off	Off
31	Off	Off	Off	Off	Off

Table 2-8: RS-232 Interface Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	Shield GND	14	(Spare)
2	RXD	15	(Spare)
3	TXD	16	(Spare)
4	RTS	17	(Spare)
5	CTS	18	(Spare)
6	DSR	19	(Spare)
7	Signal GND	20	DTR
8	(Spare)	21	(Spare)
9	(Spare)	22	(Spare)
10	(Spare)	23	(Spare)
11	(Spare)	24	(Spare)
12	(Spare)	25	(Spare)
13	(Spare)		(Spare)

Table 2-9: Dipswitch Settings for RS-232 Baud Rate

BAUD RATE	SWITCH		
	6	7	8
110	On	On	On
150	Off	On	On
300	On	Off	On
600	Off	Off	On
1200	On	On	Off
2400	Off	On	Off
4800	On	Off	Off
9600	Off	Off	Off

In addition to the IEEE-488 interface, there is also a connector on the rear panel of the receiver which contains discrete, dedicated status and control lines intended for interfacing to various associated hardware. The signals on the various connector pins are listed in table 2-10.

Table 2-10: Status/Control Output Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	Signal GND	14	Unlock
2	Front Overload	15	Back Overload
3	Underload	16	AC High
4	AC Low	17	DC Unregulated
5	Spare Power Status	18	Control 0
6	Control 1	19	Control 2
7	Control 3	20	Control 4
8	Control 5	21	Control 6
9	Control 7	22	Control 8
10	Control 9	23	Control 10
11	Control 11	24	Control 12
12	Control 13	25	Control 14
13	Control 15		

2.11 Ground Stud

A very good ground connection is necessary for the receiver to perform within specification, especially at low frequencies. A ground stud is provided on the rear panel for this purpose. consisting of a 1/4 - 20 bolt and nut. It is recommended that a large, braided ground strap be connected from the stud to a cold-water-pipe or a copper stake driven at least eight feet into the ground. If the receiver is to be used in a system consisting of several pieces of hardware, then a common ground plate should be used to connect ground straps from all instruments in a star configuration, with the pipe or stake connection then being made to the plate.

2.12 Preparation for Reshipment

If at all possible, all shipments of the R-110 should be made in the original factory container. When a new instrument is unpacked, all packing material should be retained for this purpose. Packing the instrument for reshipment should be performed as follows.

Reshipping Procedure:

1. Remove all external cables from the instrument.
2. Enclose the instrument in a plastic bag. Tape the bag shut.
3. Place packing material in the bottom of a suitable shipping container.
4. Place the bagged receiver in the shipping container and cover with the remaining packing material. Make sure that there is adequate padding around the sides of the instrument as well.
5. Seal the box with plastic or paper tape.
6. Make sure that the container bears a label indicating that it contains fragile electronic equipment.
7. Commercial shipment should be insured.

SECTION 3. OPERATING INSTRUCTIONS

3.1 Introduction

This section provides instructions for the operation of the receiver. The section begins with identification of the various controls, pushbuttons, displays, indicators, and connectors. The modes of operation and the default settings are then presented, along with a list of condensed operating instructions. More detailed discussions follow, providing an in-depth understanding of the receiver's operational features.

3.2 Identification of Controls, Displays, and Connectors

Figure 3-1 is a front view of the receiver with numerical designators that are referenced to the identification list of table 3-1. Figure 3-2 provides a back view of the instrument and is referenced to the nomenclature listed in table 3-2. The tables provide a short explanation of function and purpose for each designated item; more detailed explanations are given later.

3.3 Modes of Operation

The primary modes of operation of the R-110 are "Tune", "Scan", "MDC", and "Remote":

Tune: The normal mode of operation. In this mode the receiver is tuned using the rotary tuning control (29), the pushbuttons (14), or the keypad (11). The TUNE mode indicator (23) is illuminated.

Scan: In scan mode the receiver automatically scans a preset frequency range, using preselected step size, rate, and repetition parameters. The SCAN mode indicator (23) is illuminated.

MDC: In this mode the R-110 is connected to a model R-1180 microwave downconverter via the IEEE-488 interface. The R-110 controls the interface and commands the downconverter. The downconverter is placed in remote mode and is set via the R-110's front panel controls. The R-110 remains in tune, scan or other local operating mode. R-110 operation is affected as follows:

- RF input #1 (1) is dedicated to the downconverter output.
- The RF input select pushbuttons (7, 8) are used to control the input selection of the MDC.
- The RF input attenuation of the receiver is set to a fixed value.
- The RF input attenuation pushbuttons (9) are used to control the input attenuation of the downconverter.
- The tuning range of the radio is extended to 18 GHz.
- The MDC mode indicator (24) is illuminated.

Remote: In this mode the R-110 is under control of a host computer. Control is accomplished via the IEEE-488 interface. The REMOTE mode indicator (23) is illuminated.

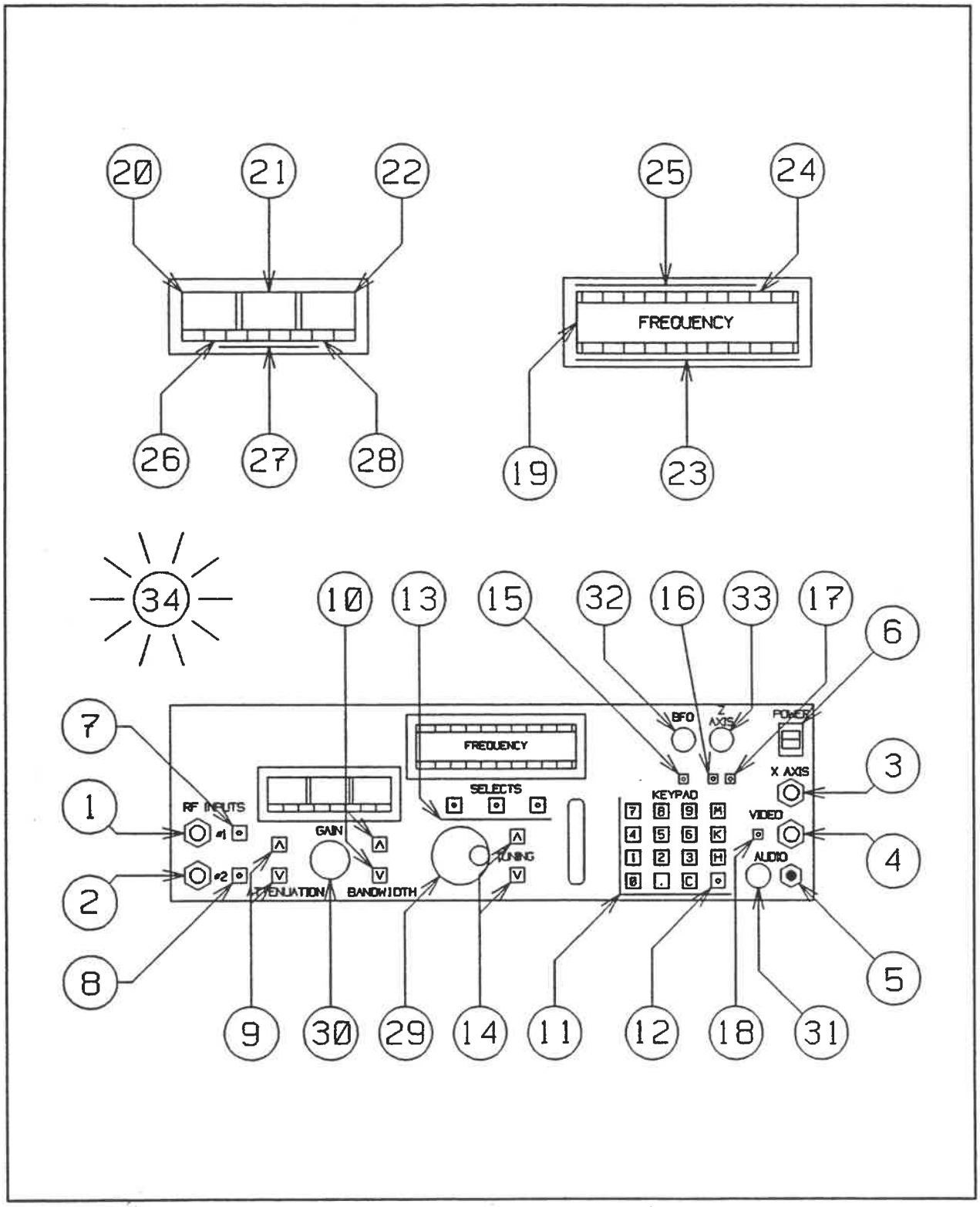

Figure 3-1: Front Panel Reference Designations

Table 3-1: Front Panel Nomenclature

Designation	Description	Designation	Description
1	RF Input #1 Connector	18	Log Pushbutton
2	RF Input #2 Connector	19	Tuning Display
3	X Axis Output Connector	20	Attenuation Display
4	Video Output Connector	21	Gain Display
5	Audio Output Connector	22	Bandwidth Display
6	Power Switch	23	Operating Mode Indicators
7	RF Input #1 Pushbutton	24	MDC Indicator
8	RF Input #2 Pushbutton	25	Status Indicators
9	RF Input Attenuation Pushbuttons	26	Autorange Indicator
10	IF Bandwidth Pushbuttons	27	Gain Mode Indicators
11	Keypad	28	External Wideband Indicator
12	Alternate Function Pushbutton	29	Frequency Tuning Control
13	Select Pushbuttons	30	IF Gain Control
14	Tuning Pushbuttons	31	Audio Volume Control
15	BFO Pushbutton	32	BFO Tuning Control
16	Z Axis Enable Pushbutton	33	Z Axis Level Control
17	Z Axis Invert Pushbutton	34	Audible Indicator

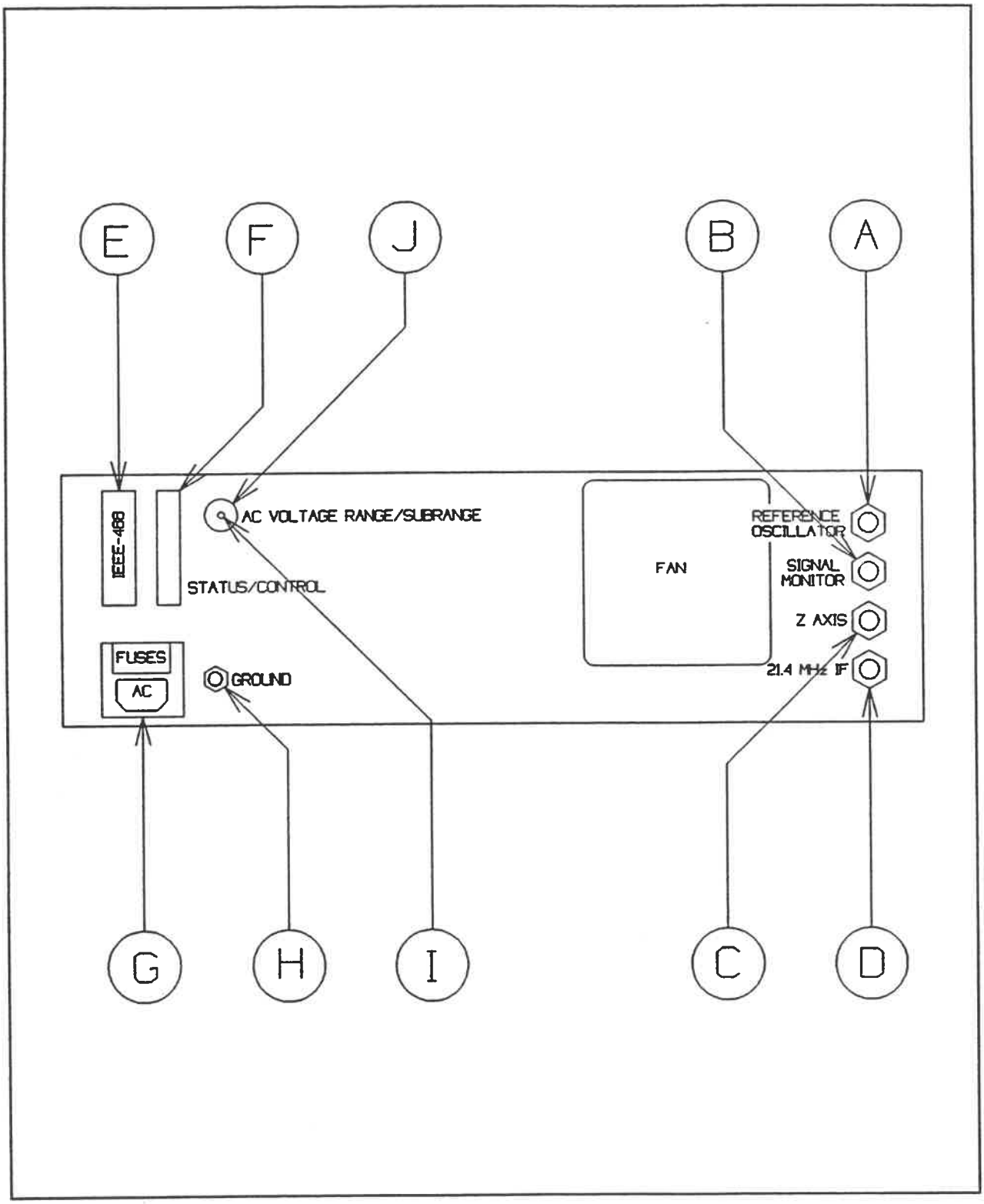

Figure 3-2: Rear Panel Reference Designations

Table 3-2: Rear Panel Nomenclature

Designation	Description
A	Reference Oscillator Output Connector
B	Signal Monitor Output Connector
C	Z Axis Output Connector
D	21.4 MHz IF Output Connector
E	IEEE-488 Interface Connector
F	Status/Control Output Connector
G	AC Line Connector / Fuse Holder
H	Ground Stud
I	AC Voltage Range Switch
J	AC Voltage Subrange Switch

In addition to these primary operating modes, additional, secondary operating modes are provided for entry of parameters and control of functions not directly provided by the front panel controls, including selection of display brightness and beep loudness, storage and recall of panel settings, AGC selection, attenuation, gain, and bandwidth modes, and IEEE-488 interface address display and temporary selection.

The modes are summarized in the condensed procedures in paragraph 3.5 and discussed in detail in paragraph 3.7.

3.4 Default Settings

When the receiver is first powered up, default operating modes and settings are automatically selected, and the front panel indicators and displays are set accordingly. These defaults are stored in reprogrammable memory and may be changed by the user using the "store settings" operating mode. The default conditions provided by the factory are listed in table 3-3.

Table 3-3: Default Settings

Parameter	Setting
Operating Mode	Tune
Tuned Frequency	100 MHz
Tuning Digit Selection	1 MHz
RF Input Selection	RF #1
RF Input Attenuation	20 dB
IF Gain	50 dB
IF Bandwidth	1 MHz
BFO	Disabled
Z Axis Output	Disabled
X Axis Output	0 Volts
Video Output	Linear
Autorange	Disabled
AGC	Disabled
Frequency Tuning	Stepped From Display Digit
Gain Mode	Impulsive Distribution, Knob Display
Bandwidth Mode	Normal, Narrowband
Scan Start Frequency	1 KHz
Scan Stop Frequency	1 GHz
Scan Step Size	100 Hz
Scan Rate	1 Step/Second
Scan Repeat Mode	Single Scan
MDC Control	Disabled
IEEE-488 Interface Address	Preset
Display Brightness	Preset
Front Panel Beep Volume	Preset
Audio Beep Volume	Preset
Audible Indicator Mode	Limit Indication Only

3.5 Condensed Operating Instructions

PRIMARY OPERATION:

Prepare for use:	Verify that the AC voltage range switch (I) is properly set. Verify that the receiver RF input connectors (1)(2) are not connected to a high voltage/energy source (e.g. a PLISN). Connect an IEEE-488 interface cable if remote or downconverter operation is intended.
Power the receiver:	Turn on power switch (6). The receiver will power up and will apply its default settings.
Select tuned frequency:	Enter a frequency (with decimal point) using keypad (11), followed by H, K, or M (Hz, kHz, or MHz).
Step tuned frequency:	Select a tuning resolution display digit with the select pushbuttons (13) and tune using the tuning knob (29) or pushbuttons (14).
Select RF input:	Press the RF Input #1 (7) or #2 (8) pushbutton.
Select RF input attenuation:	Use the RF input attenuation pushbuttons (9) and display (20).
Set IF gain:	Use the IF gain knob (28) and display (21).
Select IF bandwidth:	Use the bandwidth pushbuttons (10) and display (22).
Monitor audio output:	Connect a headphone or speaker to the audio output jack (5).
Adjust audio volume:	Use the audio volume control (31).
Monitor video output:	Connect a cable to the video output connector (4).
Select video detector:	Use the log detector pushbutton (18).
Monitor unprocessed IF:	Connect a cable to the signal monitor output connector (B).
Monitor processed IF:	Connect a cable to the 21.4 MHz IF output connector (D).
Monitor Z-axis output:	Connect a cable to the Z-axis output connector (C) on the rear panel; activate the Z-axis output by pressing the enable pushbutton (16); select polarity with the invert pushbutton (17).
Adjust Z-axis output:	Rotate the Z axis output level control (33).
Tune BFO:	Press the BFO pushbutton (15) to enable it; rotate the BFO tuning control (32) while monitoring the audio output to for tuning.

SECONDARY OPERATION:

Select Autorange: Press the alternate function pushbutton (12) followed by the keypad (11) AGC mode select key (the "3" key); use the lefthand select pushbutton (13) to select autorange. Observe the autorange mode indicator (26).

Select AGC: Press the alternate function pushbutton (12) followed by the keypad (11) AGC mode select key (the "3" key); use the righthand select pushbutton (13) to select the AGC function. Observe the AGC mode indicator (27).

Select gain display: Press the alternate function pushbutton (12) followed by the keypad (11) gain mode select key (the "2" key); use the lefthand select pushbutton (13) to select the desired gain display mode. Observe the absolute and delta gain mode indicators (27).

Select gain distribution: Press the alternate function pushbutton (12) followed by the keypad (11) gain mode select key (the "2" key); use the righthand select pushbutton (13) to select the desired gain distribution. Observe CW gain distribution indicator (27).

Select bandwidth mode: Press the alternate function pushbutton (12) followed by the keypad (11) bandwidth mode select key (the "." key); use the select pushbuttons (13) to select the desired bandwidth mode. Observe the external wideband mode indicator (28).

Select tuning step mode: Press the select step pushbutton (13) to select the stored step size as the increment/decrement value in tune mode; press the alternate function pushbutton (12) followed by keypad (11) step mode key ("4" key); then enter the desired step size; press the select step pushbutton to select ramped tuning upon return to tune mode.

Store panel settings: Press the alternate function pushbutton (12) followed by the keypad (11) store mode key (the "9" key); use the select pushbuttons (13) to select temporary, permanent, or powerup storage; enter the storage location number on the keypad; then press the H key to store the settings.

Recall panel settings: Press the alternate function pushbutton (12) followed by the keypad (11) recall mode key (the "6" key); use the select pushbuttons (13) to select temporary, permanent, or powerup storage; enter the storage location number on the keypad; then press the H key to recall the settings from storage.

Set IEEE-488 interface: Press the alternate function pushbutton (12) followed by the keypad (11) IEEE-488 mode key (the "C" key); use the left- and righthand select pushbuttons (13) to select MDC mode or remote control, and the center select pushbutton to enable/disable them; enter desired MDC or IEEE-488 address on the keypad followed by the H key to enter; use the tuning knob (29) or pushbuttons (14) to step the displayed address selection up or down.

Select Display Brightness: Press the alternate function pushbutton (12) followed by the keypad (11) brightness mode key (the "M" key); use the select pushbuttons (13) to select the desired display brightness; the selected brightness level will be stored in nonvolatile memory and will be applied at subsequent powerups as well.

Select Beeper Level: Press the alternate function pushbutton (12) followed by the keypad (11) beep mode key (the "K" key); use the select pushbuttons (13) to select beep mode and level functions; for beep level adjustments use the tuning knob (29) and pushbuttons (14) to adjust the desired beep level through the audio output connector (5) or front panel beeper (34).

Reset the receiver: Press the alternate function pushbutton (12) followed by the keypad (11) reset mode key (the "C" key) to enter reset mode; use the select pushbuttons (13) to select the desired reset function; use the keypad (11) H key to trigger the selected reset.

SCAN OPERATION:

Enter start frequency: Press the alternate function pushbutton (12) followed by the keypad (11) start mode key (the "0" key); enter the start frequency on the keypad.

Enter stop frequency: Press the alternate function pushbutton (12) followed by the keypad (11) stop mode key (the "1" key); enter the stop frequency on the keypad.

Enter step size: Press the alternate function pushbutton (12) followed by the keypad (11) step mode key (the "4" key); enter the step size on the keypad.

Enter step rate/repeat mode: Press the alternate function pushbutton (12) followed by the keypad (11) rate mode key (the "5" key); enter the step rate on the keypad (0 for maximum rate, uncalibrated); use the left- and righthand select pushbuttons (13) to select unidirectional, bidirectional, or no repetition; use the select step pushbutton to select continue or revert after pause.

Control scan: Press the alternate function pushbutton (12) followed by the keypad (11) scan mode key (the "8" key); use the select pushbuttons (13) to scan from start to stop (scan up key) or from stop to start (scan down key).

Adjust scan: During a scan, use the select pushbuttons (13): press the scan down pushbutton when scanning up to slow down the scan, or the scan up pushbutton to speed up. Press the scan up pushbutton when scanning down to slow down the scan, or the scan down pushbutton to speed up.

Pause scan and tune: During a scan, press the scan pause pushbutton (13) to temporarily halt the scan; use the tuning knob (29) or the tuning pushbuttons (14) to manually tune within the range of the scan start and stop frequencies, with steps equal to the scan step size. Press the scan up or scan down pushbutton to continue the scan in the indicated direction, or press the scan pause pushbutton again to continue the scan in the previously selected direction. Continuation will be from the last scan frequency if "revert" is selected, or from the currently tuned frequency if "continue" is selected.

Monitor X-axis output: Connect a monitoring device to the X-axis output connector (3); the output linearly tracks the progress of an ongoing scan.

Return to tune mode: Press the alternate function pushbutton (12) followed by the keypad (11) tune mode key (the "7" key) to resume tuning at the frequency at which the scan was terminated.

STATUS INDICATORS (25):

AC HI: Indicates that the AC line voltage is too high; check the AC voltage range switch (I); change the AC voltage subrange switch (J) to the next higher setting.

AC LO: Indicates that the AC line voltage is too low; check the AC voltage range switch (I); change the AC voltage subrange switch (J) to the next lower setting.

REG: Indicates that one or more of the DC supplies is out of regulation; check if the AC LO indicator is illuminated; if not then the receiver needs service.

UNLOCK: Indicates that one or more of the LO synthesizers is unlocked; flashes occasionally when tuning; if the indicator remains continuously illuminated then the radio needs service.

FR OVL: Indicates a front end overload: flashes for short overloads; for long overloads, increase the RF input attenuation.

BK OVL: Indicates a back end IF, DCIF, and/or video overload: flashes for short overloads; for long overloads decrease the IF gain setting.

BW LIM: Indicates that the tuned frequency is less than twice the selected bandwidth; decrease the bandwidth setting.

BW GAP: Indicates that the selected tuning step size is greater than the selected bandwidth, resulting in gaps in coverage when tuning; decrease the tuning step size or increase the bandwidth setting.

3.6 Detailed Operating Instructions

The following paragraphs describe the various receiver functions and their associated operational procedures. The reference numbers in the text are defined in tables 3-1 and 3-2, and are shown in figures 3-1 and 3-2.

The receiver includes audible indicators which sound when an operational limit is exceeded, or when an error condition or hardware fault is detected. A piezo transducer (34) is provided behind the front panel, and a beep tone is injected into the audio (headphone) output (5). Conditions which cause the indicators to sound are noted in the descriptions.

3.6.1 RF Input Pushbuttons, Indicators, and Connectors

The user may select one of two available RF inputs. Each input is provided with a connector (1)(2) on the front panel. Next to each connector is a pushbutton switch (7)(8), and in the middle of each button is an indicator LED. In order to select an input the operator presses the adjacent pushbutton. When this is done the pushbutton's LED will be illuminated and the LED of the other pushbutton extinguished, with the illuminated LED indicating the selected input. The input selection is also a remotely controllable function, with selection via the IEEE-488 interface; the appropriate indicator LED will be illuminated to show which input is currently selected. When in remote mode the pushbuttons will have no effect. In MDC mode the #1 input of the receiver is always selected, and the pushbuttons may be used to select the downconverter's input. When MDC mode is terminated, either by tuning the receiver below 1 GHz or by disabling the function entirely, input selection returns to that made before activating the MDC. When exiting remote mode, any selection made in that mode will be maintained until changed by the operator using the pushbuttons.

3.6.2 RF Input Attenuation Pushbuttons, Indicator, and Display

The user may select one of eight available RF input attenuation settings from 0 dB to 70 dB in 10 dB steps; the selected attenuation is shown on the four-character alphanumeric input attenuation display (20) in dB, for example "30dB". Selection is made by means of a pair of pushbuttons (9), one with an "up" arrow and the other a "down" arrow. Pressing the up arrow button increases the attenuation by 10 dB while pressing the down arrow decreases it by 10 dB. When an attempt is made to go below 0 dB of attenuation then the selection will stay at 0 dB and the audible indicator will sound. When an attempt is made to go above 70 dB of attenuation then the selection will stay at 70 dB and again the audible indicators will sound. Holding down one of the pushbuttons will cause the selection to step automatically after a short delay.

The autorange function makes use of the RF input attenuator. When this function is enabled the pushbuttons which normally control input attenuation are disabled. Instead, front end overload and underload signals are used to step the attenuator up and down to place the signal amplitude within the optimum range. When autorange is enabled the attenuation setting is shown on the display in parentheses, for example "(30)". The autorange indicator (26) is also illuminated. Autorange and its control are discussed in paragraph 3.7.10.

RF input attenuation is settable over the IEEE-488 interface. When in remote mode, autorange is disabled and the last selected value of attenuation is maintained until changed by an IEEE-488 interface command. In remote mode the up and down arrow pushbuttons are disabled, but the display will indicate all new selections made over the bus. When remote is terminated the last attenuation setting will be maintained until the operator changes it with the arrow pushbuttons. The autorange function is unavailable in remote.

In MDC mode the receiver's input attenuation is set to a fixed value and the control pushbuttons are used to set the input attenuation of the downconverter. The attenuation display will still indicate the setting of the R-110, however. If autorange is enabled in MDC mode then the downconverter's input attenuation is allowed to vary in response to its overload status signal, but the R-110's input attenuation remains fixed.

3.6.3 IF Gain Control, Indicators, and Display

User-controlled IF gain is settable over a 50 dB range, using the IF gain control (30) and the its display (21). Use of the IF gain control causes adjustments to be made in several places in the radio's signal path. The IF gain control is a high-resolution shaft encoder, while the IF gain display provides four alphanumeric characters. The display indicates the set gain value only to the nearest dB, but the adjustment granularity is about ten times smaller.

Rotating the control clockwise increases the gain in the 21.4 MHz IF, while rotating it counterclockwise reduces it. When the end of the adjustable range is reached the final value will be maintained and the audible indicators will sound.

The four characters of the IF gain display normally show the knob setting in dB, for example "12dB".

IF gain is affected by AGC, when enabled. A slowly varying voltage representative of signal level in the video output is routed back to some of the gain control stages in the 21.4 MHz IF, producing a feedback loop which tends to normalize the video output. When AGC is enabled, the setting of the front panel gain control is partly superceded, and so the displayed gain value is the knob setting shown in parentheses, for example "(30)". AGC and its selection are discussed in paragraph 3.7.10. When AGC is in use the front panel gain control should be set to maximum for the AGC to have full effect.

There are two kinds of options available for gain, one for distribution and one for display. Gain distribution may be optimized for either impulsive or CW signals. While either may be selected using a keypad function, the defaults are impulsive gain distribution for normal operation and CW distribution when the BFO is enabled. A gain mode indicator (27) illuminates when CW gain distribution is selected.

The IF gain display normally indicates the setting of the IF gain control knob. The other available gain display modes are "absolute" and "delta". In absolute mode the total gain through the receiver is shown, including the effects of the RF input attenuator, the IF gain control, and bandwidth compensating gain. The gain is displayed in dB as a signed integer. The value may be negative for high attenuation, low IF gain control setting, and wide bandwidth. Delta mode is similar except that the displayed value is calculated relative to the gain at the time that delta display mode was enabled. In other words, the display is initialized to zero when the mode is entered and incremented or decremented by changes in RF input attenuation, IF gain control setting, or IF bandwidth setting. The display is similar to that used for absolute display mode. When one of these modes is selected the associated gain mode indicator (27) will illuminate. When AGC is enabled its display supercedes those of the delta and absolute modes, since gain can no longer be indicated precisely.

Selection of gain options is discussed in paragraph 3.7.8.

Gain is a remotely controllable function. The same resolution that is available to the control is available over the IEEE-488 interface, but again the display only indicates it to the nearest 1 dB. When in remote mode the IF gain control knob is disabled, while the display updates on any settings made over the interface. The IF gain is displayed in the same format as knob gain, and if AGC is enabled the display will be similar to the display in local. When remote operation is terminated the last setting made is maintained until the operator changes it with the front panel gain control. In MDC mode the IF gain control operates as usual.

3.6.4 Bandwidth Pushbuttons, Indicator, and Display

Receiver IF bandwidth is selected using a pair of pushbuttons (10), one with an up arrow and the other a down arrow. The display (22) consists of four alphanumeric characters. The indication is given in digits and a multiplier, for example "300k". Pressing the up arrow key selects the next broader available bandwidth while pressing the down arrow key selects the next narrower available bandwidth. When an attempt is made to exceed the broadest or narrowest available bandwidth then the selection will be maintained and the audible indicators will sound. Holding down one of the arrow keys will cause selection to step repeatedly after a short delay.

The default set of bandwidths are those most commonly used, following a 1-2-5 sequence in the range covered by the DCIF. Since the DCIF is capable of providing many more bandwidths than this an expanded set may be selected using the keypad. Selection is discussed in paragraph 3.7.9. Once selected, operation of the bandwidth pushbuttons and the format of the display remain the same. The expanded set is selected so as to provide to make the noise normalization for each successive bandwidth increase by 1 dB per step.

Another available option, selected by the same means as the extended bandwidth selection mode, is external wideband mode. When selected, this mode routes the output of the 1450 MHz IF to a connector on the top of the microwave RF module in the cardcage, bypassing the 21.4 MHz IF, the video, and the audio. In this mode the bandwidth pushbuttons are disabled, the display indication is "EXT!" and the external wideband mode indicator (28) is illuminated. Tuning resolution is only to 5 MHz, and frequencies below 15 MHz are unavailable. The IF gain display (21) is also disabled. Bandwidth in this mode is about 200 MHz.

In MDC mode there is no change in the operation of the IF bandwidth controls or display.

IF Bandwidth is a remotely controllable function. When in remote mode the arrow pushbuttons are disabled. The display, however, is updated when bandwidth commands are received, so the display remains current. When remote mode is terminated the current bandwidth is maintained until the operator changes it with the pushbuttons.

3.6.5 Tuning Control, Pushbuttons, and Display

Tuning controls include the keypad (11), the tuning knob (29), the tuning pushbuttons (14), and the select pushbuttons (13). The tuning display (19) consists of twelve alphanumeric characters. The normal frequency display consists of digits and a decimal point, with a multiplier on the right-hand end, for example "100.00000MHz". Displayed resolution changes with the frequency to be displayed and can range from 0.1 Hz to 10 Hz.

Absolute tuning is accomplished by means of the keypad. The operator may enter digits and optionally a decimal point, followed by a terminator consisting of "M" for MHz, "K" for kHz, or "H" for Hz, depending on the way the digits and decimal point were entered. For example, a frequency of 1 MHz could be entered as "1M" or "1.000M" or "1000K" or "1000000H". If an error is made during the entry the "C" key may be pressed to clear it. Digits and the decimal point are presented on the frequency display as they are entered. Pressing a terminator key causes the entry to be evaluated and the nearest legal value accepted, set into hardware, and displayed in the standard format.

Stepped tuning is accomplished by means of the tuning knob and pushbuttons, and by the select pushbuttons. One digit of the tuning display may be selected for stepping by means of the left and right select pushbuttons. Pressing the left button advances the digit selection to the left, while the right pushbutton advances it to the right. In either case the selection will wrap around to the other end of the display if one button or the other is pressed enough times in succession, with one null selection intervening. Holding down either button will cause selection to step automatically after a short delay. The decimal point and multiplier characters, and also leading blanks, may not be selected.

A selected display digit will blink. This will be the digit referenced by the tuning knob anad pushbuttons. If a situation occurs in which a new frequency is set (e.g., via the keypad) for which the previously selected tuning digit is unavailable, then the decimal point will blink to indicate the condition. Stepping resolution remains that which was previously selected. An example of this is tuning the radio to 100 MHz, selecting the MHz digit for tuning, and then setting the radio to 10 kHz via the keypad. Since the MHz digit is unavailable for blinking, the decimal point is caused to blink instead.

Rotating the tuning knob clockwise will step the frequency upward, using the selected frequency display digit as the reference for step size. Similarly, rotating the knob counterclockwise will step the frequency downward. For example, if the display character representing the MHz digit of the frequency is selected, then the step size will be 1 MHz. Pressing the tuning pushbutton marked with an up-arrow will cause the frequency to increase by one step. Similarly, pressing the button marked with a down arrow will cause the frequency to decrease by one step. Holding either button down will cause the frequency to step repeatedly in the indicated direction after a short delay.

Pressing the center select pushbutton (marked "STEP") will cause the selection of a display digit to be cancelled. Instead, the stored step size specified as one of the scan parameters is used. When this mode is enabled the indicator LED inside the STEP pushbutton is illuminated. Tuning is otherwise the same as when a display digit is selected. Pressing the STEP button again will return to normal operation, as will pressing either of the arrow select buttons.

Entry of a stored step size is described in paragraph 3.7.5.

If the tuned frequency is less than twice the selected bandwidth then the BW LIM status indicator indicator (25) will illuminate and the audible indicator will sound. If the selected tuning step size is greater than the selected bandwidth then the BW GAP status indicator will illuminate.

One additional tuning option pertains to the manner in which frequency tuning is stepped up or down. In the default operating mode the step is made in a single jump, from the old frequency to the new one, subject to the speed at which the receiver's microprocessor can make all of the necessary hardware settings. At certain combinations of tuned frequency, step size, and selected bandwidth, operation in this mode can cause clicking in the audio, due to the sudden change in output level. The option, called "ramped tuning", causes tuning which under some circumstances might produce the clicking to be performed more gradually, with up to 16 microsteps per tune step. While this effectively changes the click to a buzz, the audible level of the buzz is theoretically lower since the change of output level between microsteps is smaller.

Ramp tuning may be selected as part of stored step size entry mode, as described in paragraph 3.7.5. Operation with the option enabled is considerably slower than normal when the tuned frequency, step size, and bandwidth selections make it most useful, but has no perceptible effect on operating speed otherwise.

In MDC mode both the downconverter and the receiver are tuned simultaneously. The necessary coarse resolution frequency is sent to the downconverter and the frequency appropriate to tune the desired frequency within the output of the downconverter is set into the receiver. In this mode both the receiver and the downconverter will display the tuned frequency rather than the frequencies actually set into them. When downconverter mode is exited the true tuned receiver frequency will be displayed.

In remote mode the tuned frequency may be set over the IEEE-488 interface. In addition, a step size may be entered and commands issued to step frequency up and down. When remote mode is exited the last frequency setting made will be maintained until changed manually by the operator.

3.6.6 Video Selection and Output

The video output (4) can be taken from either a log or a linear detector, with linear being the default selection. The LOG pushbutton (18) toggles selection between them. An indicator LED in the pushbutton illuminates when the log detector is selected.

Both the linear and the log detector may be selected in remote mode, but not the BFO. The linear detector is generally used. In remote mode the LOG pushbutton is disabled, but if the selection is changed by a bus command then the LED will be updated to indicate the current selection. When remote is exited any changes made while in remote will be maintained until the operator changes the selection again with the pushbutton.

3.6.7 Audio Output and Volume Control

The audio output (5) will drive headphones or a speaker, or any reasonable load down to a few Ohms. The audio volume control (31) sets the gain. At the counterclockwise end of the control's rotation there is zero output, while at the other end the output will be about 50 times the amplitude provided by the video circuit. The audio output signal includes an audible warning "beep" when an operational limit is exceeded; adjustment of this level is discussed in paragraph 3.7.14.

The input of the audio circuit is provided by an output of the video circuit. Since the gain for a given bandwidth is set to normalize the noise at the video output, in cases where the video bandwidth is greater than the audio range the noise in the audio output will not be normalized for different bandwidths. In effect this makes for quieter audio output at wider bandwidths. In addition, for CW or voice-type signals, there is greater apparent loudness at narrower bandwidths for any given setting of receiver and audio gain. This is the case regardless of whether impulsive or CW gain distribution is selected.

When BFO operation is selected the audio circuit monitors the BFO output rather than that of the video circuit. The video output remains normal, however. BFO operation is described in paragraph 3.6.8 below.

There is no control of the audio circuit available in remote mode, except that since BFO is likewise not controllable in remote, audio input selection reverts to the output of the AM detector in remote. In MDC mode the circuit functions normally.

3.6.8 BFO Control, Pushbutton, and Indicator

The BFO ("beat frequency oscillator") is used to detect unmodulated (or nearly so) CW signals. If the BFO is set to a slight deviation from the IF frequency then a "beat frequency" occurs at a frequency equal to the difference between the two. This beat frequency may be heard through the audio output connector (5). The BFO is settable over a +/- 4 kHz range by the BFO control (32). The associated pushbutton (15) is used to enable/disable the function. BFO takes the place of the normal AM detection link to the audio output, so that pressing the button to enable BFO takes the AM detector output off of the audio circuit. Pressing the pushbutton again restores the AM detector and turns off the BFO. A LED indicator located in the pushbutton illuminates when BFO is selected and is extinguished otherwise. Selection of BFO has no effect on the video output.

BFO is not a remotely settable or selectable function, and is disabled in the remote mode. It stays off when remote mode is exited, so the operator must then press the button to reselect it if it is desirable to do so. The button is disabled during remote mode. In MDC mode the circuit functions normally.

3.6.9 Z Axis Output Control, Pushbuttons, and Indicators

The Z axis output (C) is similar to the video output, but is located on the rear panel and has different controls. The output is provided to drive the Z axis (intensity) input of an oscilloscope. The Z axis control (33) adjusts the level, the polarity pushbutton (17) inverts the signal, and the select pushbutton (16) turns the output on and off. LEDs in the pushbuttons illuminate to indicate the state, with "on" and "inverted" cases producing illumination. When the transition from "off" to "on" is made, the last polarity set since powerup is selected. The powerup default polarity is normal.

The Z axis function is not remotely controllable. It is automatically disabled when entering remote. Operation in MDC mode is normal.

3.6.10 Signal Monitor and 21.4 MHz IF Outputs

There are two other signal outputs on the rear panel of the receiver, taken from two different points in the signal path. The first (B) is the signal monitor output, which is picked off of the 21.4 MHz IF before the gain control and bandwidth filtering stages. Full tuning resolution and range are available, and bandwidth is fixed at about 20 MHz, subject to the constraints of the input stages for the various tuning bands.

The second (D) is the 21.4 MHz IF output, taken this time from the same point which drives the DCIF and video sections, following the first gain control stage and the bandwidth filters. Again full tuning range and resolution are available, but now bandwidths down to 80 KHz are available, along with partial gain control.

3.6.11 Reference Oscillator Output

This rear-panel output (A) provides external monitoring and use of the receiver's internal reference clock. The frequency is 20 MHz, divided from the oscillator's 100 MHz, and the amplitude is -10 dBm.

3.6.12 X Axis Output

The X axis output (3) produces a 0 to +10 Volt ramp signal during programmed scans. It is provided to drive the horizontal input of an oscilloscope or X axis input of a plotter, to implement spectral presentations. It has no associated controls or indicators. The output is nonzero only during scan operations. At the start of a scan the output is set to 0 Volts and progresses in linear steps to +10 Volts at the stop frequency. Further discussion of scans is provided in paragraph 3.7.7.

The X axis output is unused in remote mode. Operation in MDC mode is normal.

3.6.13 Status Indicators

The status indicators (25) are alphanumeric indicators located in the upper portion of the tuning display window. Indicators are provided for synthesizer, overload, and power supply status, as well as for bandwidth and tuning step size selection errors. Lock status, overload, and power supply status is also available at the rear panel status connector and over the IEEE-488 interface.

The "AC HI" indicator illuminates when AC line voltage is too high for the current power supply input voltage selection. Change the line voltage range to the next higher setting using the subrange switch (J) on the rear panel. An AC high condition should not normally damage the radio unless it has inadvertently been switched to 117 VAC operation and used with a 220 VAC line. This condition is beyond the ability of the subrange switch to cope with and will almost certainly damage the radio.

The "AC LO" indicator illuminates when AC line voltage is too low for the current power supply input voltage selection. Change the line voltage range to the next lower setting using the subrange switch (J) on the rear panel. If the "REG" indicator is also illuminated in conjunction with the AC LO indicator then the line voltage is too low to be usable, given that the subrange switch is already in the LOW position.

The "REG" indicator illuminates when one or more of the power supply regulators is out of tolerance. It can be caused by the power line being out of tolerance (indicated by the "AC LO" indicator), or a problem in the receiver.

The "LOCK" indicator illuminates when one or more of the synthesizer's phase locked loops (PLLs) is out of lock. When all PLLs are in lock the indicator is extinguished. If one PLL is out of lock for just an instant the lightbar will give a quick flash. If the lightbar stays on the radio must be serviced.

The "FR OVL" indicator illuminates when an RF overload is detected. Detection is placed at the start of the 21.4 MHz IF, before the settable gain stages. For a short overload it gives a flash. For a long overload the input attenuation must be increased.

The "BK OVL" indicator illuminates when a 21.4 MHz IF, DCIF, or video overload is detected. For a short overload it gives a flash. For a long overload the IF gain setting must be decreased.

The "BW LIM" indicator illuminates when the selected IF bandwidth is greater than half of the tuned frequency. This is beyond what the hardware can cope with and will produce an erroneous output from the receiver. See paragraph 3.6.4.

The "BW GAP" indicator illuminates when the selected tuning step size is greater than the selected IF bandwidth, which will allow gaps in tuning coverage. For either continuous manual tuning or scanning the step size should always be less than the bandwidth.

3.7 Alternate Keypad Functions

Some receiver functions are selected and/or controlled using the keypad (11). Since the primary function of the keypad is to enter tuned frequencies, these other functions are called "alternate". They are accessed by pressing the alternate function pushbutton (12) which is placed in the lower righthand corner of the keypad layout. Pressing the alternate function pushbuttons will cause its internal indicator LED to illuminate to indicate that an alternate selection is pending. Pressing it again will cancel the pending condition and extinguish the indicator.

Once accessed, alternate keypad functions may be thought of as small-scale operating modes, in which the functions of the tuning display (19), the select pushbuttons and indicators (13), the keypad, and the tuning knob (29) and pushbuttons (14), are re-assigned to different uses. A chart of the use of these controls in each keypad-selected operating mode is given in table 3-5. The remaining front panel controls, indicators, and displays remain unaffected, save as a result of selection in one of these modes (e.g., absolute gain display mode, once selected, will change the IF gain display).

The keypad keys have their alternate functions printed above them. When an an alternate function is made pending using the alternate function pushbutton, any other keypad key may subsequently be pressed to access its designated alternate function.

A list of alternate functions is given in table 3-4.

Table 3-4: Alternate Keypad Functions

Keypad Key	Function
7	Tune Mode
8	Scan Mode
9	Store Settings Mode
M	Display Brightness Adjustment Mode
4	Scan Step Size Entry Mode
5	Scan Rate Entry Mode
6	Recall Settings Mode
K	Audible Indicator Control Mode
1	Scan Stop Frequency Entry Mode
2	Gain Options Select Mode
3	AGC Select Mode
H	IEEE-488 Interface Control Mode
0	Scan Start Frequency Entry Mode
.	Bandwidth Options Select Mode
C	Reset Select Mode

All of the alternate functions will be discussed in the following paragraphs.

3.7.1 Mode Indicators

There are ten mode indicators (23) located along the bottom of the tuning display (19) window. Indicators are provided for tune mode, start frequency entry mode, stop frequency entry mode, step size entry mode, scan rate entry mode, scan mode, store settings mode, recall settings mode, IEEE-488 interface control mode, and remote operating mode. All of these modes are mutually exclusive, so that only one of these indicators may be illuminated at any time. When one of the remaining alternate function modes is selected (display brightness selection mode, audible indicator amplitude setting mode, gain option selection mode, bandwidth option select mode, or AGC selection mode) all ten of the indicators are extinguished. In these cases the operating mode can be determined from the message on the tuning display.

3.7.2 Tune Mode

Tune mode is the default primary mode of operation of the receiver. Tune mode is entered from the other keypad-selectable modes by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated, and then pressing the keypad (11) key with "TUNE" marked above it (the "7" key). The TUNE mode indicator (23) will illuminate while the indicator LED in the alternate function pushbutton will be extinguished.

In this mode the tuned frequency is shown on the tuning display. Tuned frequencies may be entered via the keypad, or stepped by means of the tuning knob (29) and pushbuttons (14), with step resolution selected by the select pushbuttons (13). The procedure for entering parameters via the keypad is described in paragraph 3.6.5.

Two different methods of selecting tuning step size are available. Firstly, the STEP select pushbutton (13) may be pressed to select the stored step size (entered in step size entry mode, described in paragraph 3.7.5) as the size of each frequency step. Secondly, either the left or right select pushbutton may be pressed to select a digit of the tuning display (19) to designate the step size. See paragraph 3.6.5.

If an attempt is made to set the frequency beyond the limits of the receiver then the nearest legal setting will be substituted and the audible indicators will sound. When a step is generated using the tuning knob or pushbuttons which is beyond the limits of the receiver, the step is rejected and the existing value retained.

3.7.3 Start Frequency Entry Mode

Start frequency is one of the scan mode parameters, the nominal starting point of the scan. To enter this mode, first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "START" marked above it (the "0" key). The indicator LED in the alternate function pushbutton will extinguish and the START mode indicator (23) will illuminate. The tuning display (19) will show the last stored start frequency. The keypad digit and terminator keys may now be used to enter any start frequency from 1 kHz to 1 GHz. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered frequency will be stored for use by scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or when the receiver is reset.

3.7.4 Stop Frequency Entry Mode

Stop frequency is one of the scan mode parameters, the nominal end point of the scan. To enter this mode first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "STOP" marked above it (the "1" key). The indicator LED in the alternate function pushbutton will extinguish and the STOP mode indicator (23) will illuminate. The tuning display (19) will show the last stored stop frequency. The keypad digit and terminator keys may now be used to enter any stop frequency from 1 kHz to 1 GHz. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered frequency will be stored for use by scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or when the receiver is reset.

3.7.5 Step Size Entry Mode

Step size is one of the scan mode parameters, but it may also be used as the step size for normal tuning in tune mode. To enter this mode first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "STEP" marked above it (the "4" key). The indicator LED in the alternate function pushbutton will extinguish and the STEP mode indicator (23) will illuminate. The tuning display (19) will show the last stored step size. The keypad digit and terminator keys may now be used to enter any step size from 0.1 Hz to 1 GHz. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered value will be stored for use by tune mode or scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or the receiver reset.

Selection of stepped vs. ramped tuning is also made in this mode. The STEP select pushbutton (13) is used to toggle the selection. After pressing the pushbutton the new selection will be indicated on the tuning display. Ramped tuning is slower than stepped, since it breaks up the tuning step into a number of microsteps when the overall step is large in comparison to selected bandwidth. The purpose of ramped tuning is to reduce clicking in the audio due to sudden changes in output level resulting from relatively large shifts in tuned frequency. In practice the click is replaced by a chirp, but at a lower amplitude.

3.7.6 Scan Rate Entry Mode

This mode is used to set the scan rate, the scan repeat mode, and the action on resumption of a scan after a pause. To enter it first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "RATE" marked above it (the 5 key). The indicator LED in the alternate function pushbutton will extinguish and the RATE mode indicator (23) will illuminate. The tuning display (19) will show the last stored scan rate. The keypad digit and terminator keys may now be used to enter any scan rate from 0.01 to 10.00 steps per second. Alternatively a rate of zero may be entered to scan at the maximum possible (but uncalibrated) scan rate (about 25 steps per second). An illegal rate will be replaced by the nearest legal one. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered value will be stored for use by scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or the receiver reset.

Scan repetition mode is set using the left- and righthand select pushbuttons (13). Pressing either button selects, in sequence, either no repetition (single scan), unidirectional repetition, or bidirectional repetition. Unidirectional repetition repeats a scan beginning again at the initial frequency, whereas bidirectional repetition scans back and forth between the endpoints.

The center select pushbutton selects the scan resumption after pause option. Since manual tuning is possible during a scan pause, the tuned frequency when a scan is continued may not be the same as when the pause was initiated. Pressing the center select button to select the "CONTINUE" option will cause the scan to resume from the current frequency, whereas selecting the "REVERT" option will cause the scan to continue from where it left off. After pressing the select button the currently selected option will be shown on the tuning display.

3.7.7 Scan Mode

Scan mode is used to automatically step through a sequence of frequencies, using preselected values for start frequency, stop frequency, step size, step rate, and repetition. All of these are initialized to default values at powerup, but it is usually necessary to set each of them to desired values before commencing a scan. Each entry is made in a secondary operating mode, as described in the preceding paragraphs.

Scan mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "SCAN" marked above it (the 8 key). The indicator LED in the alternate function pushbutton will extinguish while the SCAN mode indicator (23) will illuminate. The tuning display (19) will indicate the currently tuned frequency.

In scan mode the three select pushbuttons (13) are used to control the scan. The pushbuttons are given an alternate set of designations (printed below them) for this purpose. In this mode the pushbuttons are labeled "SCAN DOWN" (the left pushbutton), "SCAN PAUSE" (the center pushbutton), and "SCAN UP" (the right pushbutton). If a scan is not currently in progress, then pressing the SCAN UP pushbbutton will initiate a scan from the start frequency to the stop frequency. Pressing the SCAN DOWN pushbutton will initiate a scan from the stop frequency to the start frequency. Upon reaching the end of its range, the scan will either halt, reverse itself, or start over, depending upon the setting of the scan repeat mode. The indicator LED inside whichever pushbbutton is pressed will illuminate while the scan is running.

If a scan is running, then pressing the same pushbutton used to initiate the scan will cause it to speed up, up to the maximum executable rate of about 25 steps per second. Pressing the opposite pushbutton will cause the scan to slow down. Each press will cause the rate to approximately double or halve, respectively.

Pressing the SCAN PAUSE pushbutton while a scan is running will cause the scan to be suspended but not cancelled. Pressing the pushbutton again will cause it to resume. Alternatively, pressing either the SCAN UP or SCAN DOWN pushbuttons during a pause will cause the scan to resume in the desired direction.

During a pause the indicator LED in the SCAN PAUSE pushbutton will illuminate. At this time the tuning knob (29) and pushbuttons (14) may be used to step the frequency manually, using the scan step size as the increment or decrement. The tuning range is limited to the range of the scan. Ramped tuning is unavailable in this mode.

Resumption of the scan after a pause may be made from either the currently tuned frequency or from the frequency at which the pause was initiated. Selection of either option is made in the same submode in which scan rate and repetion mode is selected.

When not scanning or paused the radio may be tuned normally using the keypad, tuning knob, and tuning pushbuttons, using the stored step size as the tuning resolution.

3.7.8 Gain Options Select Mode

There are two kinds of gain option selections available, one for gain distribution and one for gain display. Distribution can be optimized for either impulsive or CW signals, impulsive being the factory-set default for normal operation and CW being the default when the BFO is enabled. The IF gain display can indicate either the gain control knob setting, or the total gain of the radio, or gain relative to a reference level, in which changes in input attenuation and bandwidth-compensating gain are also tracked. For a discussion of these options see paragraph 3.6.3.

The mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "GAIN" marked above it (the "2" key). The indicator LED in the alternate function pushbutton will extinguish while the tuning display (19) will indicate the currently selected gain options. No mode indicator (23) will be illuminated.

Selections are made using the select pushbuttons (13). The lefthand pushbutton selects the display mode while the righthand pushbutton selects the distribution mode. The center pushbutton selects the default combination of both. Both modes are indicated on the tuning display simultaneously, the display mode on the left and the distribution mode on the right. In addition, when CW gain distribution, or absolute or delta gain display mode is selected, the appropriate gain mode indicator (27) will illuminate.

Gain display selection depends on whether or not AGC is enabled. If enabled, the AGC mode gain display will supercede the selection made with the select pushbuttons.

Gain distribution selection depends on whether or not BFO is enabled. The selections with BFO enabled and disabled are independent, as are the defaults. Changing the BFO selection may change the gain distribution selection as well.

All options are available in MDC mode. Only gain distribution selection is available in remote mode, though not from the front panel.

3.7.9 Bandwidth Options Select Mode

More bandwidths are available than those provided in the default selection. To make all of them selectable an extended bandwidth selection option is provided. All of these extra bandwidths are at the narrow end of the range, provided by the DCIF. At the wide end, a wideband selection is available for future expansion. If selected, the tuning range of the radio will be limited to 15 MHz at the low end, the tuning resolution will be limited to 5 MHz steps, and the signal path will be truncated after conversion to the 1450 MHz IF. See paragraph 3.6.4 for more discussion.

The mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "BW" marked above it (the "." key). The indicator LED in the alternate function pushbutton will extinguish while the tuning display (19) will indicate the currently selected bandwidth option. No mode indicator (23) will be illuminated.

Selections are made using the select pushbuttons (13). Only one option may be selected at any given time. The left and right pushbuttons step through the selections, while the center pushbutton causes selection to revert to the default condition. When external wideband mode is selected the WIDE indicator (28) will illuminate.

All options are available in MDC mode. Extended narrowband selection is the normal case in remote mode, and external wideband mode is available as well, though it is not selectable from the front panel in remote.

3.7.10 AGC Select Mode

There are two sorts of automatic gain control (AGC) available. The first sort, called autorange, reacts to the signal amplitude at the front of the 21.4 MHz IF by stepping the RF input attenuator up or down. Since the RF input attenuator steps in 10 dB increments, this is a coarse adjustment. The second sort of AGC, back end AGC, reacts to the signal amplitude in the video section by adjusting the gain in the 21.4 MHz IF. This is an analog feedback and gain control with continuous and fairly rapid response, though over a slightly narrower dynamic range. Throughout this manual, the term "AGC" refers to back end AGC only. See paragraph 3.6.3 for more discussion.

When autorange is enabled the attenuation pushbuttons (9) are disabled.

When AGC is enabled the IF gain display automatically shifts to AGC display mode. This overrides any other gain display mode which may be selected, except that if external wideband mode is selected then there is no gain display at all, since the controlled gain stages are no longer in the signal path.

AGC select mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "AGC" marked above it (the "3" key). The indicator LED in the alternate function pushbutton will extinguish while the tuning display (19) will indicate the currently selection of AGC and autorange. No mode indicator (23) will be illuminated.

Selections are made using the select pushbuttons (13). The lefthand pushbutton toggles autorange on/off while the righthand pushbutton does the same for AGC. The center pushbutton selects the default condition, which in the factory-provided selection is with neither selected. The AUTO indicator (26) illuminates when the function is enabled. Likewise, the AGC indicator (27) illuminates when AGC is enabled.

Both sorts of gain control are available in MDC mode, noting that autorange will affect the input attenuation of the MDC rather than that of the R-110 when tuning is in the downconverter range. Only AGC is available in remote mode.

3.7.11 Store Settings Mode

To store the current front panel settings, first press the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "STORE" marked above it (the "9" key). The indicator LED in the alternate function pushbutton will extinguish and the STORE mode indicator (23) will illuminate. A prompt will be shown on the tuning display (19). Using the select pushbuttons (13), select the type of storage to be used: temporary, permanent, or powerup (which is also permanent). Using the keypad (11), enter the location number in which to store the settings (0 - 99) if temporary or permanent storage is selcted (this is unnecessary if powerup storage is selected). Finally, press the "H" key to store the settings. The following settings will be stored:

- Current tuned frequency
- Current scan start frequency
- Current scan stop frequency
- Current step size
- Current scan rate
- Current input selection
- Current input attenuation
- Current gain
- Current bandwidth
- Current AGC selections
- Current gain options
- Current bandwidth options
- Current tuning options
- Current scan options
- Current slideback on/off state (not the adjustment)
- Current pulse stretch on/off state (not the adjustment)
- Current BFO on/off state (not the adjustment)
- Current Z axis on/off and invert states (not the adjustment)
- Current log/lin detector selection
- Current audible indicator on/off states (not the amplitudes)
- Current MDC enable or GPIB enable

The following are NOT stored:

- Slideback threshold adjustment
- Pulse stretch adjustment
- BFO frequency adjustment
- Z axis output amplitude adjustment
- Audio output amplitude adjustment
- Audible indicator amplitudes
- Display brightness
- Current GPIB address (read from dipswitch at powerup)
- Current MDC address (not expected to change often)

Once the operation has been completed a message will be provided on the tuning display indicating whether the settings were stored in temporary or permanent memory.

3.7.12 Recall Settings Mode

Most of the front panel control settings may be recalled from previous storage and set into hardware. This is the companion function to the store settings mode described in the previous paragraph, and operation is similar.

To recall stored control settings, first press the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "RECALL" marked above it (the "6" key). The indicator LED in the alternate function pushbutton will extinguish and the RECALL mode indicator (23) will illuminate. A prompt will be shown on the tuning display (19). Using the select pushbuttons (13), select the type of storage to be accessed: temporary, permanent, or powerup. Using the keypad (11), enter the location number from which to recall the settings (0 - 99). Finally, press the "H" key to perform the recall. For powerup storage only the terminator is needed. The following settings will be recovered and set into hardware:

- Current tuned frequency
- Current scan start frequency
- Current scan stop frequency
- Current step size
- Current scan rate
- Current input selection
- Current input attenuation
- Current gain
- Current bandwidth
- Current AGC selections
- Current gain options
- Current bandwidth options
- Current tuning options
- Current scan options
- Current slideback on/off state (not the adjustment)
- Current pulse stretch on/off state (not the adjustment)
- Current BFO on/off state (not the adjustment)
- Current Z axis on/off and invert states (not the adjustment)
- Current log/lin detector selection
- Current audible indicator on/off states (not the amplitudes)
- Current MDC enable or GPIB enable

The following are NOT recovered:

- Slideback threshold adjustment
- Pulse stretch adjustment
- BFO frequency adjustment
- Z axis output amplitude adjustment
- Audio output amplitude adjustment
- Audible indicator amplitudes
- Display brightness
- Current GPIB address (read from a dipswitch at powerup)
- Current MDC address (not expected to change often)

Once the operation has been completed the tuned frequency will be shown on the tuning display. About one second later a message will be provided on the tuning display indicating whether the settings were read from temporary or permanent memory.

If a location is read in which no data was previously stored then the default powerup settings will be read and set into hardware.

3.7.13 Display Brightness Selection Mode

The alphanumeric displays (19)(20)(21) are capable of four brightness levels, one of which is "off". To change the current brightness setting, press the alternate function pushbutton (12) so that the indicator LED located inside is illuminated. Then press the keypad (11) key with "BRIGHT" marked above it (the "M" key). The indicator LED in the alternate function pushbutton will extinguish and a mode message will appear on the tuning display (19), assuming that "off" is not already selected. No mode indicator (23) will be illuminated. The select pushbuttons (13) may now be used to step the selected brightness level. Note that only the brightness of the alphanumeric displays is affected, not that of the status indicators (25) or mode indicators (23)(26)(27)(28), and not that of the indicator LEDs located inside some of the pushbuttons. The selected brightness level is stored in nonvolatile memory so that it will be read and restored even after power is cycled.

3.7.14 Audio Indicator Selection and Adjustment Mode

There are two audible indicators. One is a piezo transducer (34) located behind the front panel, while the other is a feed into the audio output circuit. The amplitude of each may be adjusted independently. In addition, various triggers for the indication may be switched on and off.

To enter the adjustment mode press the alternate function pushbutton (12) so that the indicator LED located inside is illuminated. Then press the keypad (11) key with "BEEP" marked above it (the "K" key). The indicator LED in the alternate function pushbutton will extinguish and the tuning display (19) will show a mode status message. No mode indicator (23) will be illuminated. The left and right select pushbuttons (13) may now be used to select the desired beep function. Beep triggers consist of the following:

- Limit beep. Indicates the end of a control range. For example, rotating the gain control past the 50 dB position. This produces a short beep.

- Error beep. Indicates an unacceptable keypad entry. For example, entering a tuned frequency below 1 KHz. This produces a long beep.

- Fault beep. Indicates a lock status, overload, or DC regulation fault. This produces a repeating beep which persists for the duration of the fault.

Each of the preceding may be individually switched on or off as a trigger source to the indicator, using the center select button.

The amplitude of the beep at the transducer or the audio output may be adjusted by first selecting the level adjustment mode for the desired beep type using the select keys, and then using the tuning knob (29) and pushbuttons (14) to select the desired level. The final value will be stored in permanent memory and will be re-established each time the radio is powered up. One indicator or the other may be effectively turned off by decreasing its level to inaudibility.

3.7.15 MDC Mode

MDC mode allows automatic control of a model R-1180 microwave downconverter using the IEEE-488 interface. In this mode the R-110 becomes the interface controller, commanding the downconverter and reading back status. The R-110 allows control of the downconverter's RF input selection, RF input attenuation, and tuned frequency using the R-110's front panel controls. The tuned frequency and RF input attenuation of the R-110 is automatically adjusted to the output range of the downconverter. RF input #1 (1) of the R-110 is dedicated to the downconverter output, with the other input still available for frequencies below the downconverter's range.

Two connections are required between the downconverter and the R-110. A signal cable with response to 1 GHz is used to connect the downconverter output to RF input #1 (1) on the R-110. An IEEE-488 interface cable must also be connected between the units.

Once the MDC is connected, the R-110 must also be made aware of it. This is done in IEEE-488 interface control mode. To enter this mode press the alternate function pushbutton (12) so that the indicator LED located inside is illuminated. Then press the keypad (11) key with "GPIB" marked above it (the "H" key). ("GPIB" stands for "General Purpose Interface Bus", another name for the IEEE-488 Interface.) The indicator LED in the alternate function pushbutton will extinguish and GPIB mode indicator (23) will illuminate. The tuning display (19) will show a mode status message. The left or right select pushbuttons (13) may now be used to select the MDC mode status message. Then press the center select pushbutton so that MDC operation is enabled and the presumed MDC address is displayed.

The interface address of the MDC may now be entered using the keypad or the tuning knob (29) and pushbuttons (14). If the keypad is used then the desired address should be keyed in, followed by the "H" key as a terminator. The address will be stored in nonvolatile memory and will be recalled on powerup.

Tune mode may now be reselected. No communication with the MDC will occur until the R-110 is tuned above 1 GHz. Upon exceeding 1 GHz the MDC will be placed in remote and left in remote until either it or the R-110 is switched off, or MDC mode is disabled in GPIB select mode, using the center select key. In other words, when the MDC address is displayed, MDC operation is enabled at that address. When the mode is toggled to indicate "no MDC" the mode is disabled.

Operation of the R-110 with the MDC enabled is similar to normal operations, with the following exceptions:

- RF input selection operates normally when the radio is tuned below 1 GHz. Above 1 GHz RF input #1 will be automatically selected and the RF input select pushbuttons (7,8) remotely control input selection for the downconverter. When the radio is tuned back below 1 GHz the radio's previous input selection is recalled.

- RF input attenuation operates normally when the radio is tuned below 1 GHz. Above 1 GHz a fixed attenuation is selected and shown on the attenuation display (20), while the attenuation pushbuttons (9) remotely control RF input attenuation selection for the MDC. When the radio is tuned back below 1 GHz the radio's previous input attenuation is recalled. The autorange function operates normally below 1 GHz, while above 1 GHz it remotely controls the MDC's RF input attenuator. It does this by polling the status return byte of the MDC and stepping the attenuator based on the state of the overload status bit. Since there is no matching underload status bit as is provided in the R-110, this is a fairly rudimentary form of control.

- Tuning operates normally below 1 GHz. Above 1 GHz, tuning still presents the normal interface to the operator, but will automatically determine the proper frequencies to which to tune both the radio and the MDC. The output of the MDC is in the 800 - 900 MHz range, so if an interface error occurs then the tuned frequency of the radio will revert to this range. The range of scan frequencies is extended to 18 GHz when the MDC is enabled.

- IF bandwidth selection operates normally both below and above 1 GHz. The bandwidth of the MDC is about 400 MHz, so it presents no limitation when the radio has wideband selected (the front end of the radio has about 200 MHz bandwidth).

Remote operation of the R-110 is not feasible in MDC mode. Enabling MDC mode will disable GPIB mode.

Downconverter command formats are not covered by this document, but are listed in documentation supplied with the downconverter.

3.7.16 Remote Mode

In remote mode an external host computer is in control of the receiver, using the IEEE-488 interface. In remote most of the front panel controls are disabled. Those that are still functional include:

- The power switch (6)
- The audio volume control (31)
- The BFO tuning control (32) (BFO is disabled)
- The Z axis output level control (33) (Z axis is disabled)
- The ALT pushbutton (12)
- The keypad (11) C key (when an alternate function is pending)

All displays and indicators remain functional. The only available keypad function is ALT-RESET, which returns the receiver to local if local has not been locked out.

The receiver is accessed over the IEEE-488 interface via an address which is read from a dipswitch at powerup. This dipswitch is located on the processor PCB and the procedure for setting it is given in chapter 2. While in local mode the address may be changed temporarily in IEEE-488 interface mode. See paragraph 3.7.17.

Commands are provided in remote which control:

- RF input selection
- RF input attenuation
- IF gain
- IF gain distribution
- AGC (not autorange)
- IF bandwidth, and external wideband selection
- Tuned frequency
- Tuning step size, and step up and down
- Video detector selection
- Store and recall of settings
- Status reporting

Functions which are always disabled in remote include:

- BFO
- Z axis
- X axis
- Audible indicators
- Display brightness selection
- MDC operation under control of the R-110

MDC operation is nevertheless supported, with the IEEE-488 interface host computer controlling both instruments independently.

Additional commands are provided which allow reporting of various radio settings over the bus, and for low-level control of IF gain. In addition, commands are provided which load and read back data to and from the calibration tables in the radio's nonvolatile read/write store, so that the IEEE-488 interface may be used for automated calibration.

Note that for a more efficient remotely controlled system the radio's rear panel status outputs should be connected to a separate interface in the remote system's host computer. This permits the IEEE-488 interface to remain permanently in sending mode while still monitoring status for overloads. Turning the bus around from sending to receiving is a major slowing factor for most IEEE-488-based systems.

Remote mode command formats, protocols, and supported functions are described in detail in appendix A.

3.7.17 IEEE-488 Selection Mode

The IEEE-488 interface may be used to control an external R-1180 microwave downconverter or be used to allow an external host computer to control the R-110. These two options are not available simultaneously. If a downconverter is to be employed in remote mode then it is the responsibility of the computer controlling the interface to command it. If the R-110 has control of the interface in order to command the downconverter then an external host computer will not be able to take control.

An interface address for the R-110 is read from a dipswitch on the processor PCB at powerup. This address may be changed temporarily, but the change will be lost when power is removed. It is recommended that once an address is selected it be permanently set using the dipswitches. See section 2 for the procedure.

An interface address for the external downconverter is read from nonvolatile memory on powerup. This address may be changed as well, and the new selection will be saved in nonvolatile memory.

Address and downconverter selection are performed in a keypad submode dedicated to IEEE-488 interface-related options, called GPIB mode. The mode is selected by pressing the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "GPIB" marked above it (the "H" key). The indicator LED in the alternate function pushbutton will extinguish and the GPIB mode indicator (23) will illuminate. The tuning display (19) will show a status message. The left and right select pushbuttons (13) may now be used to select MDC or GPIB control. In each case the center select pushbutton (13) may be used to toggle the selection on and off, while the keypad, tuning knob (29) and pushbuttons (14) may be used to change the displayed address when the selection is enabled. Legal addresses range from 0 to 30. When using the keypad, enter the desired address followed by the "H" key to terminate the entry, or the "C" key to revert to the old one. A new MDC address will be stored in permanent memory, whereas a new GPIB address will be held only until powerdown.

The MDC address should always be different from the R-110's own GPIB address. The R-1180 MDC comes factory-set to address 12, but this may be changed by the user. See the downconverter's documentation for details. The R-110 comes factory-set with address 16 set on the dipswitch.

This mode may be used to return an MDC to local, by setting the mode to "No MDC". When in remote this mode is unavailable, but the R-110 may be returned to local by pressing the alternate function pushbutton followed by the key with RESET marked above it ("C" key).

3.7.18 Reset Mode

Reset mode handles four sorts of resets: the IEEE-488 interface, temporary storage, permanent storage, and the entire radio.

The IEEE-488 interface reset function gets the radio off of the bus without forbidding later access. Whereas disabling both remote and MDC operation in GPIB mode (described in the preceding paragraph) will result in holding the IEEE-488 interface controller circuit in reset, using the function presented here will reset the controller and leave it in idle mode, ready to be used again. This is done by releasing control of the MDC (when MDC mode is enabled) or by returning the radio to local if it is in remote (provided local lockout has not been commanded). Note that when the radio is in remote, selecting reset mode will automatically return the radio to local without presenting the operator with the normal interface, storage, and general reset options.

Memory resets reload the selected storage with powerup data, removing any settings stored since powerup.

Resetting the entire radio reboots the control system and returns the radio to its powerup state. Note that a reset switch located on the processor PCB may also perform this function, but the pushbutton is not accessible when the radio's cover is in place.

To enter reset mode, first press the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "RESET" marked above it (the "C" key). The tuning display (19) will indicate the currently selected reset function. No mode indicator (23) will be illuminated. Use the select pushbuttons (13) to select the desired function. Then press the keypad "H" key to trigger the reset.

Table 3-5: Sub-Mode Control Functions

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Tune	Tune from selected frequency display digit	Move digit selection left with wraparound	Enter "tune stored step size" sub-mode	Move digit selection right with wraparound	Enter tuned frequency	Step tuned frequency up or down by amount of selected digit
	Tune stored step size	Enter "tune selected digit" sub-mode with selected digit one left of last	Enter "tune selected digit" sub-mode with last selected digit	Enter "tune selected digit" sub-mode with selected digit one right of last	Enter tuned frequency	Step tuned frequency up or down by amount entered in step size mode
Start					Enter scan start frequency	
Stop					Enter scan stop frequency	
Step			Toggle ramp tune option on/off		Enter scan/tune step size	
Rate		Select scan repeat option: no repeat, unidirectional, bidirectional	Toggle continue/ revert after scan pause option	Select scan repeat option: no repeat, unidirectional, bidirectional	Enter scan rate	

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Scan	Idle	Start scan stop → start		Start scan start → stop		Step tuned frequency up or down by stored step size, no start/stop limits
	Scanning towards stop	Slow down scan rate	Enter pause sub-mode	Speed up scan rate		
	Scanning towards start	Speed up scan rate	Enter pause sub-mode	Slow down scan rate		
	Pause	Restart scan towards start	Restart scan in last active direction	Restart scan towards stop		Step tuned frequency up or down by stored step size, limited to range between start & stop frequencies
Store		Select store: temp, permanent, powerup	Select default (temporary) storage	Select store: temp, permanent, powerup	Enter storage location number for temp and permanent, just "H" for powerup	

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Recall		Select store: temp, permanent, powerup	Select default (temporary) storage	Select store: temp, permanent, powerup	Enter storage location number for temp and permanent, just "H" for powerup	
Bandwidth		Select normal, extended, or wideband	Select default (normal) bandwidth	Select normal, extended or wideband		
Gain	BFO Off	Select knob, absolute, or delta display	Select defaults: knob display, impulsive distribution for no BFO only	Select impulsive or CW distribution for no BFO only		
	BFO On	Select knob, absolute, or delta display	Select defaults: knob display, CW distribution for BFO only	Select impulsive or CW distribution for BFO only		
AGC		Toggle autorange on/off	Select defaults: autorange off, AGC off	Toggle AGC on/off		
Brightness		Select display brightness down, with wraparound	Select default display brightness: full	Select display brightness up, with wraparound		

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Beep	Fault Beep	Select "panel beep level" sub-mode	Toggle fault beeps on/off	Select "error beep" sub-mode		
	Error Beep	Select "fault beep" sub-mode	Toggle error beeps on/off	Select "limit beep" sub-mode		
	Limit Beep	Select "error beep" sub-mode	Toggle limit beeps on/off	Select "beep level" sub-mode		
	Audio Beep Level	Select "limit beep" sub-mode		Select "panel beep level sub-mode		Step beep level in audio output up/down
	Front Panel Beep Level	Select "audio beep level" sub-mode		Select "fault beep" sub-mode		Step beep level in panel beep up/down
GPIB	Remote operation	Select MDC sub-mode	Toggle remote enable on/off	Select MDC sub-mode	Enter bus address if remote enabled	Step bus address up/down if remote enabled
	MDC operation	Select remote sub-mode	Toggle MDC enable on/off	Select remote sub-mode	Enter MDC address if MDC enabled	Step MDC address up/down if MDC enabled

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Reset	Reset Radio	Select "reset GPIB" sub-mode		Select "reset perm" sub-mode	"H" key triggers radio reset	
	Reset Perm	Select "reset radio" sub-mode	Select default (radio) sub-mode	Select "reset temp" sub-mode	"H" key clears permanent store	
	Reset Temp	Select "reset perm" sub-mode	Select default (radio) sub-mode	Select "reset GPIB" sub-mode	"H" key clears temp store	
	Reset GPIB	Select "reset temp" sub-mode	Select default (radio) sub-mode	Select "reset radio" sub-mode	"H" key resets GPIB controller	
Remote					Alt followed by "C" forces return to local if no lockout	

SECTION 4. THEORY OF OPERATION

4.1 Introduction

The model R-110 is a wide range superheterodyne receiver that is continuously tunable, covering the frequency range from 1 kHz to 1 GHz in three bands. See table 4-1. The receiver detects RF signals in the form of continuous wave (CW) or amplitude modulated carriers.

Table 4-1: Receiver Tuning Bands

Band	Tuning Down	Tuning Direct	Tuning Up
1	1 kHz - 224.9999 kHz	1 kHz - 249.9999 kHz	1 kHz - 264.9999 kHz
2	225 kHz - 13.4999999 MHz	250 kHz - 14.9999999 MHz	265 kHz - 16.4999999 MHz
3	13.5 MHz - 1 GHz	15 MHz - 1 GHz	16.5 MHz - 1 GHz

The breakpoints between bands for "direct tuning" are the nominal values, those which will be obtained by direct frequency entry using the keypad or IEEE-488 interface, or during scans. Hysteresis is introduced when using the tuning knob or pushbuttons, or the IEEE-488 step commands, or when tuning manually during a scan pause. This hysteresis provides the offset breakpoints shown for "tuning up" and "tuning down".

Note that when external wideband mode is selected, band 1 and band 2 are eliminated and the nominal band 3 break is the lower tuning limit of the radio whether tuning is up, down, or direct. Also, when operating in MDC mode with the external R-1180 microwave downconverter in the signal path, the tuning range inside the radio is 800 - 900 MHz. Although this falls within band 3, it is given its own designation, band 4, due to a number of special conditions that are necessary in this mode. Finally, limitations of synthesizer usage cause band 3 to be broken up into two pieces, called band 3A and band 3B. Band 3A is the first 5 MHz of band 3, regardless of where the band break occurs. This is discussed further in the description of the programmable microwave synthesizer.

The major functional parts of the receiver are:

- RF: processes RF inputs; converts to 21.4 MHz IF; implemented with three modules (A1A1, A1A2, A1A5) plus front-panel components.
- IF: performs wider bandpass filtering, AGC and programmable gain; consists of two modules (A1A6 and A1A8).
- DCIF: performs narrow-band filtering, programmable gain, and linear AM detection; implemented in a single module (A1A11).
- video: provides AM detection of wider bandwidths; provides log response; provides BFO detection; provides buffered video, Z axis, and audio outputs; implemented in a single module (A1A9).

- synthesizer: provides LO signals for frequency conversion; consists of three modules (A1A15, A1A16, A1A17) plus components in RF section.
- control: controls operation of all modules; includes front panel; contained in front panel assembly (A2A1, A2A2, A2A3).
- power supply: provides regulated power to receiver circuits using linear design to minimize EMI; contained in rear panel assembly (A3).

The simplified block diagram of figures 4-1 - 4-5 shows how the sections are interconnected (a detailed block diagram is included in section 6). The RF section uses three parallel signal paths that divide the input range into specific frequency bands, as listed in table 4-1. The signal paths contain mixer circuits used to heterodyne the tuned input signal to the 21.4 MHz intermediate frequency. The 21.4 MHz IF section provides amplification and selectable bandpass filtering. For the wider bandwidths, the 21.4 MHz IF section's output is routed to the video section which provides the audio and video output signals. For narrow bandwidths, the IF signal goes to the DCIF section where it is processed and detected.

The synthesizer section utilizes a precision direct digital synthesizer (DDS) and phase locked loop (PLL) circuits to create the required local oscillator signals, thus providing accurate frequency control and high resolution.

The power supply section of the receiver provides individually regulated DC voltages from a selection of six ranges of AC input power.

Physically, the radio consists of a front panel assembly (A2), a cardcage assembly (A1), and a rear panel assembly (A3). The front panel assembly contains the controlling microprocessor and also the RF input selection and distribution relays, and the RF input attenuator. The cardcage assembly is provided with a backplane which routes control and status signals from the front panel assembly to the various plug-in modules, and provides power to them as well. Analog and RF signal lines are routed across the tops of the modules using discrete coax cables, both flexible and semi-rigid. The rear panel assembly contains the power supply and cooling fan. The front panel assembly, cardcage assembly, and rear panel assembly bolt together to form a chassis, which may then slide into a one-piece cover, with the result being the assembled radio. Discussions following in this section will deal more or less individually with the front and rear panel assemblies, the cardcage assembly, and the various plug-in modules.

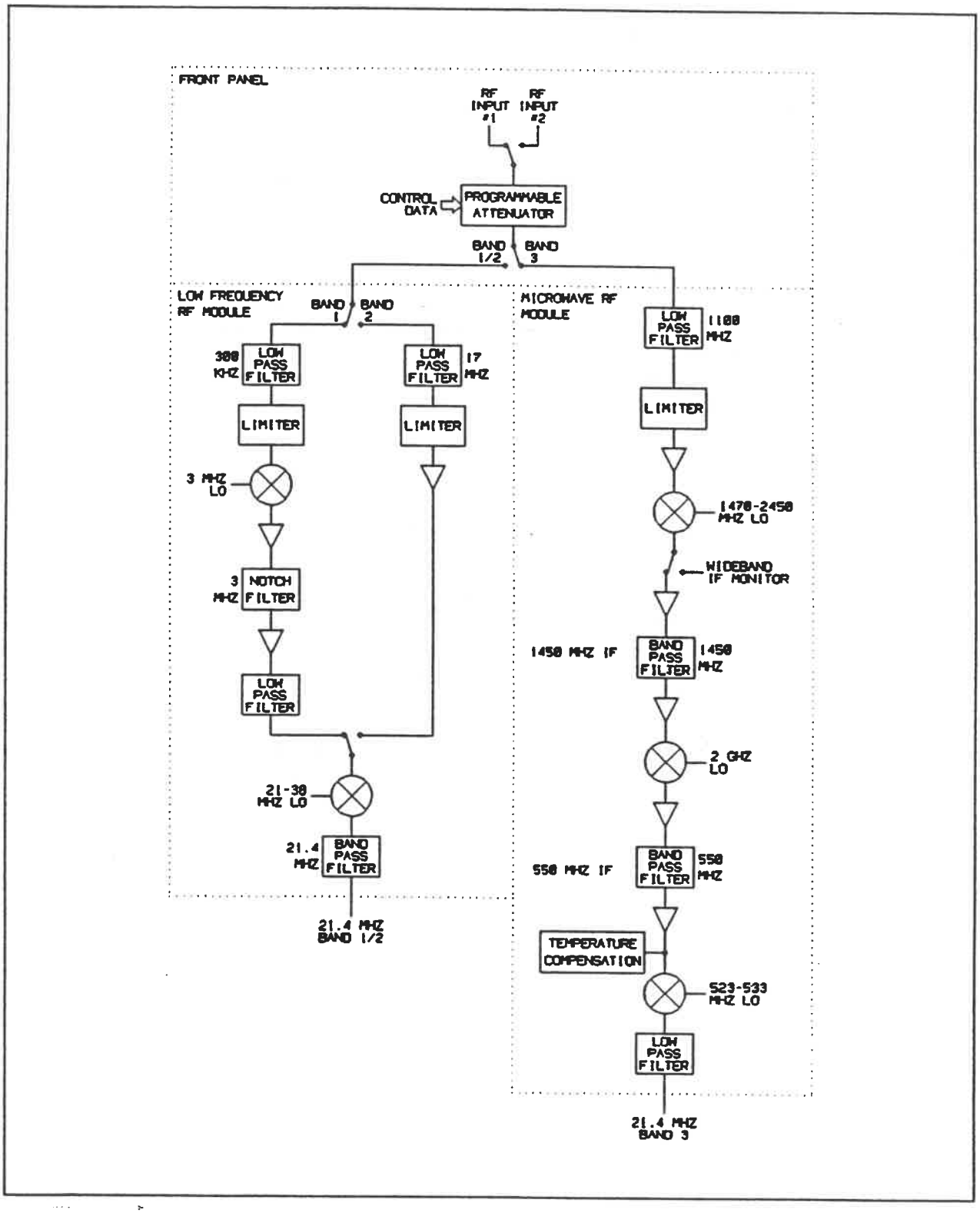

Figure 4-1: R-110 Receiver Simplified Block Diagram - Part 1

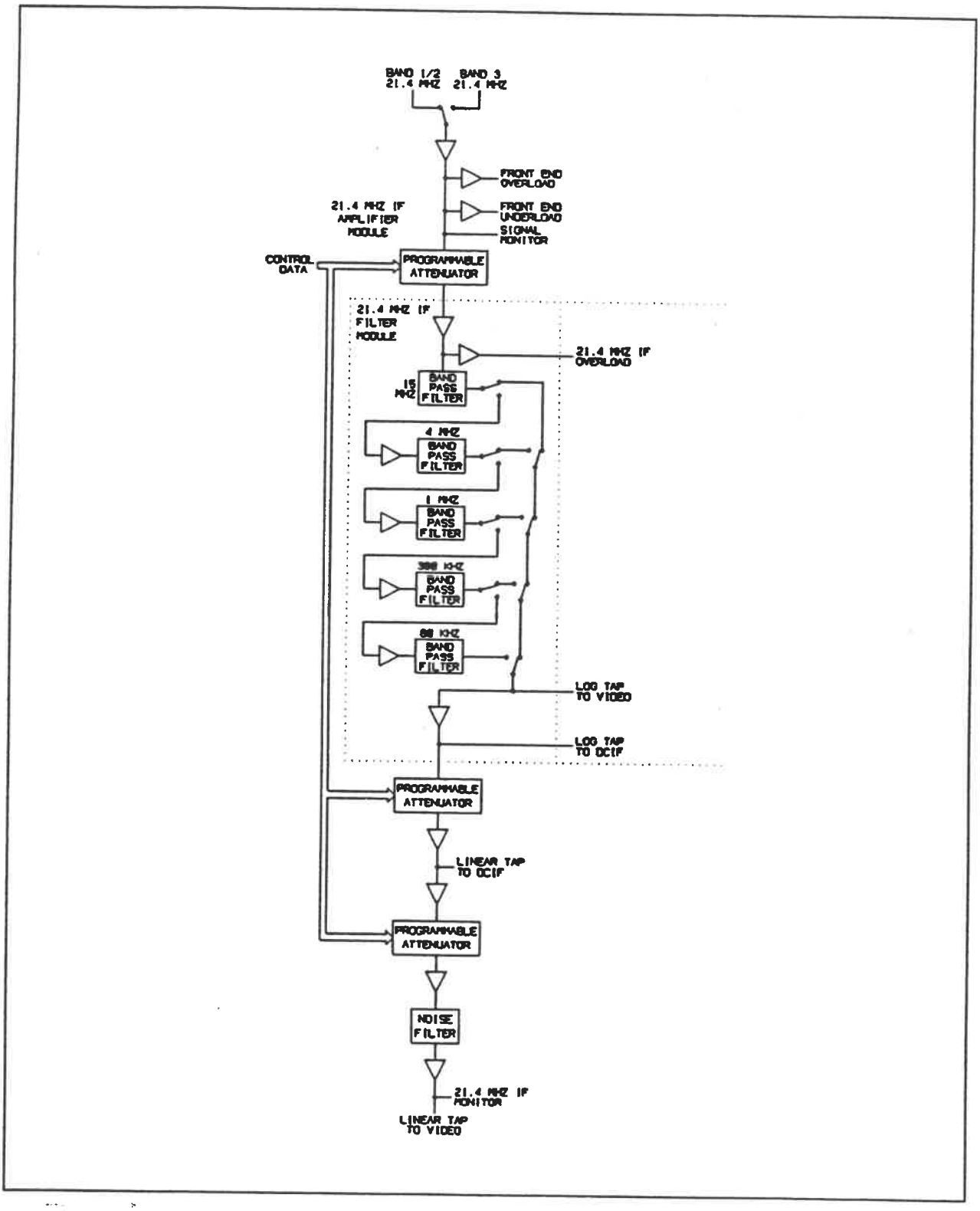

Figure 4-2: R-110 Receiver Simplified Block Diagram - Part 2

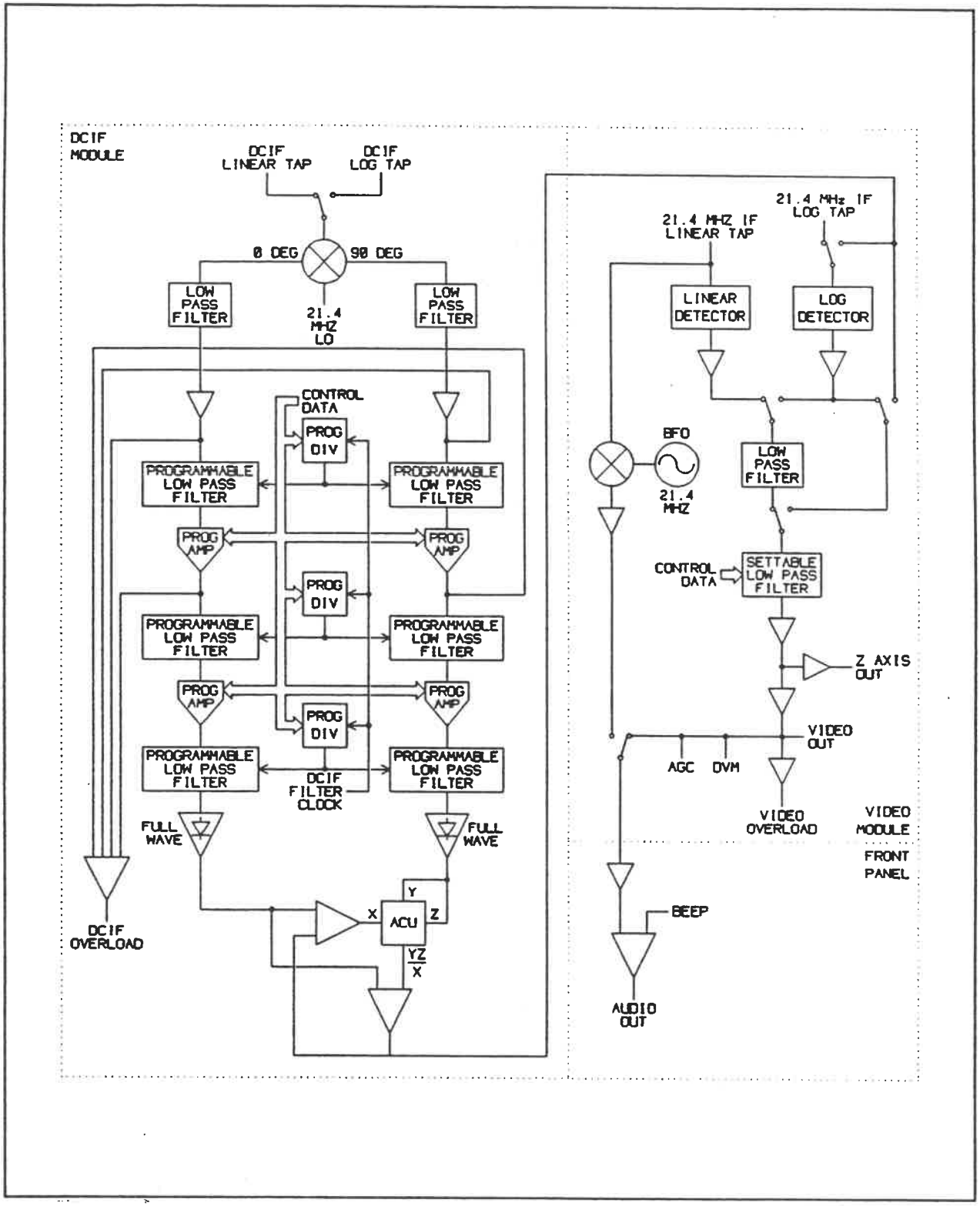

Figure 4-3: R-110 Receiver Simplified Block Diagram - Part 3

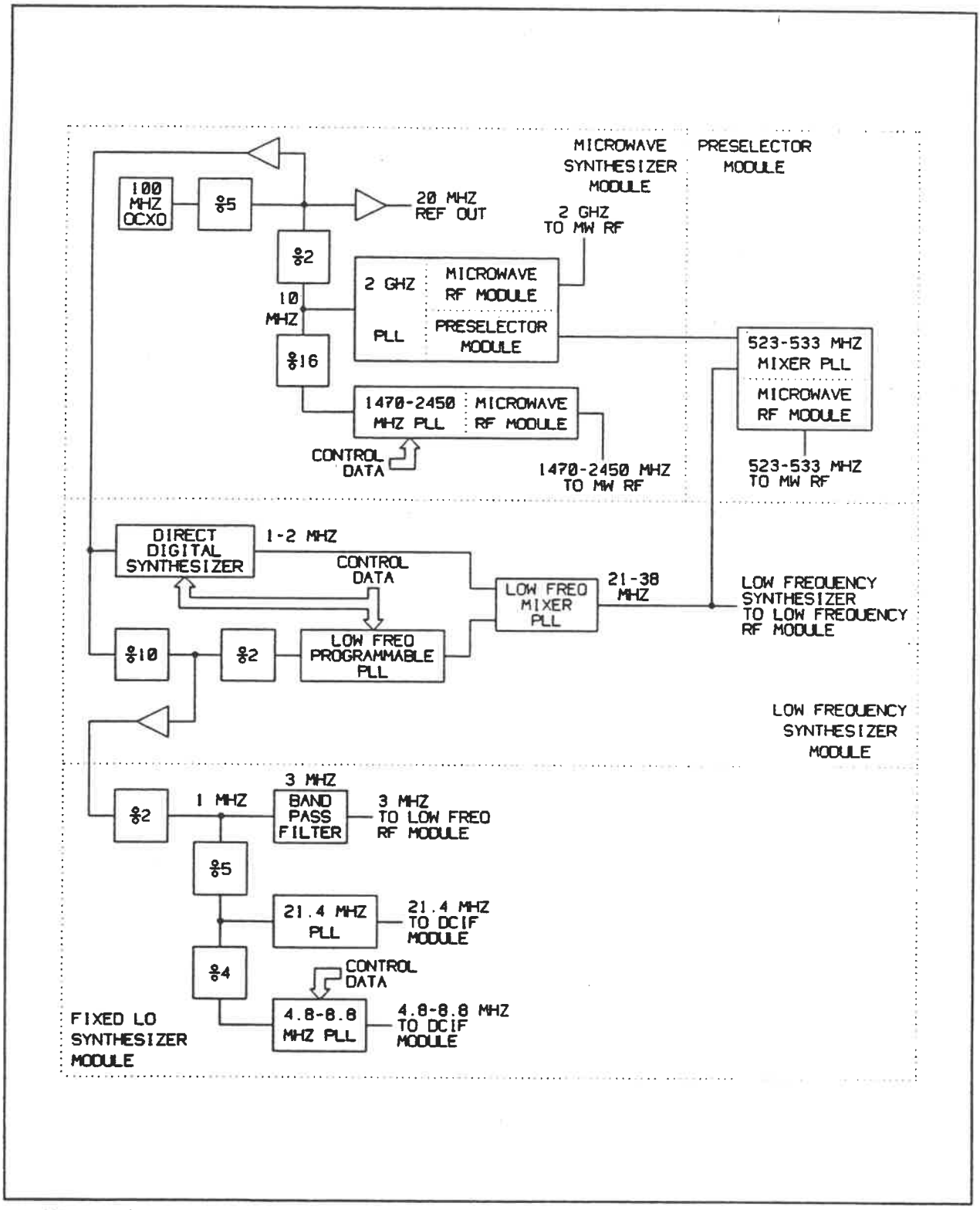

Figure 4-4: R-110 Receiver Simplified Block Diagram - Part 4

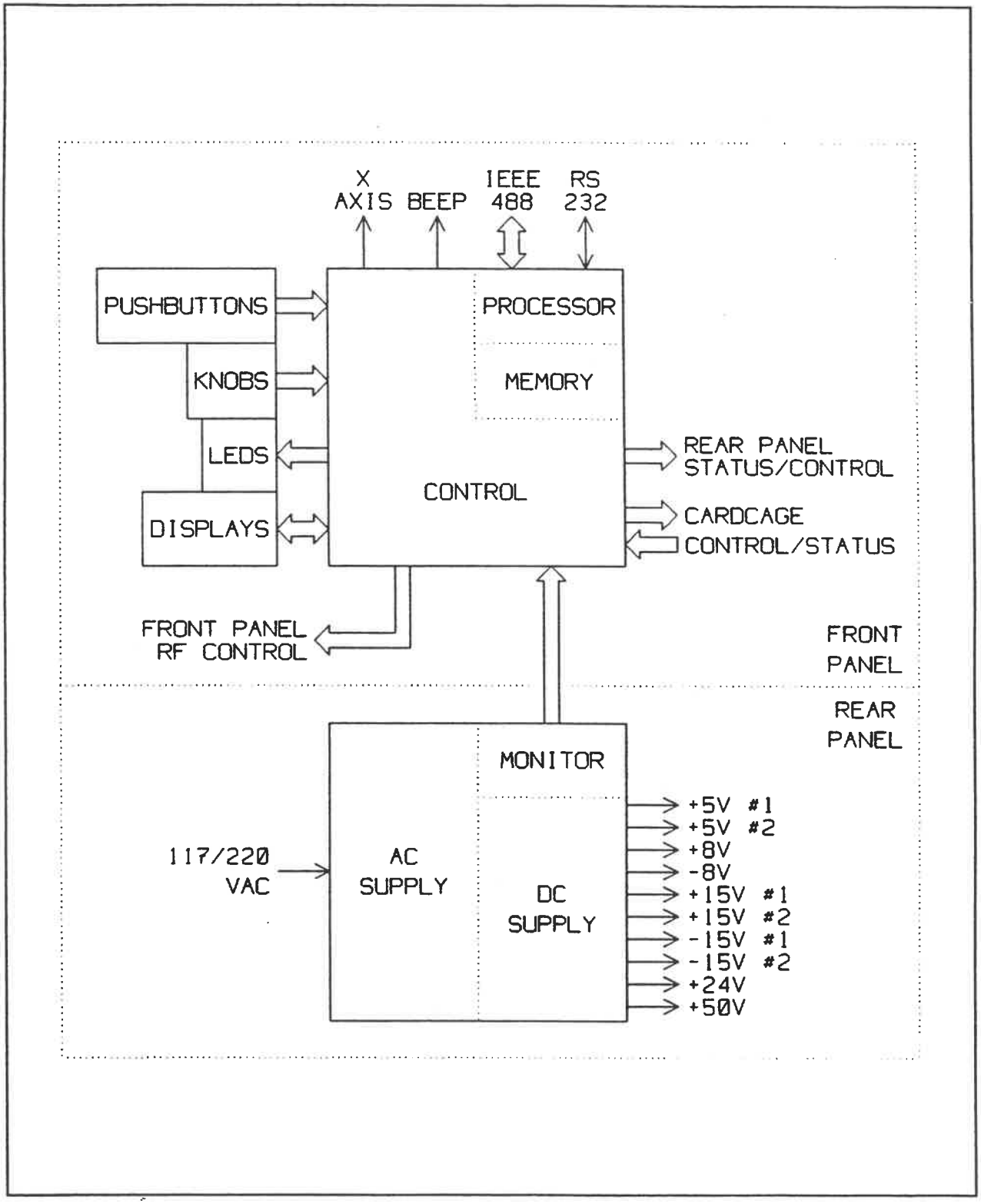

Figure 4-5: R-110 Receiver Simplified Block Diagram - Part 5

4.2 RF Section

The RF section is made up of the RF front-end components (contained in the front panel assembly), the preselector module, the microwave (MW) RF module, and the low frequency (LF) RF module.

4.2.1 Front Panel RF Components

There are two RF signal inputs to the receiver: RF input #1 and RF input #2. The two inputs are furnished with BNC connectors, which are in turn connected to a latching RF relay, which selects between them. The relay is actuated by a pulse command from the control section. The output of the relay is connected to a programmable attenuator, which ranges from 0 - 70 dB in 10 dB steps. The attenuator's controls are non-latching and are driven continuously from the control section. The attenuator's output is routed to the appropriate conversion stage by another RF relay relay which is set by the control section according to the selected tuning band. When tuning in bands 1 and 2, the signal is directed to the low frequency RF module (A1A5), while when tuning in band 3 the signal is directed to the input filter in the preselector module (A1A2). Space has been reserved for a "ground loop isolator", a device which serves to connect or disconnect input signal returns to/from chassis ground. It is currently not used in the radio, but will be necessary in the future if the tuning range of the radio is extended much below 1 kHz. While the signal input returns are currently isolated from the chassis, a hard ground is necessary when tuning low frequencies in order to reduce pickup of 60 Hz line power and its harmonics.

4.2.2 Low Frequency RF Module (A1A5)

When tuning in band 1 and band 2, the signal from the front panel RF section is passed to the low frequency RF module (A1A5) for processing and conversion. Figure 4-6 is a block diagram of the module showing the circuit functions and the LO frequencies utilized. Band 1 signals are converted to the 21.4 MHz intermediate frequency using two mixer stages. The first mixer is an up-converter that generates the sum of the band 1 received frequency and a 3 MHz fixed LO signal. The first mixer stage output is routed to a second converter where it is mixed with the output of the programmable low frequency synthesizer to produce the fixed 21.4 MHz intermediate frequency. This second converter is shared by both band 1 and band 2. Band 2 signals use only the second mixer, requiring only a single up-conversion along with the expected amplification and filtering.

At the signal input of the module (J1) is an RF relay (K1) which distributes the incoming signal from the front panel RF section to the band 1 or band 2 signal path depending on the selected tuning band (see the discussion on hysteresis at the band breaks in paragraph 4.1). The path which is not selected is terminated with 50 Ohms. The band 1 selection from the relay passes through a DC blocking capacitor (C2) and then feeds a 300 kHz lowpass filter (C6 - C11, L7, L8) which removes out-of-band signals, LO re-radiation, and image frequencies. The signal then passes through a limiter (CR3, CR4) for protection against transient spikes. The limited signal from the output of the lowpass filter drives a double-balanced mixer (U2). The other input of the mixer is fed by a 3 MHz fixed frequency LO, which arrives at -3 dBm from the synthesizer section via a coax connector (J2), and is stepped up to +7 dBm by an amplifier (U4). Since the mixer is used for up-conversion, the mixer RF and IF connections are reversed from the usual practice in order to allow the low frequency portions of the band 1 tuning range to pass through.

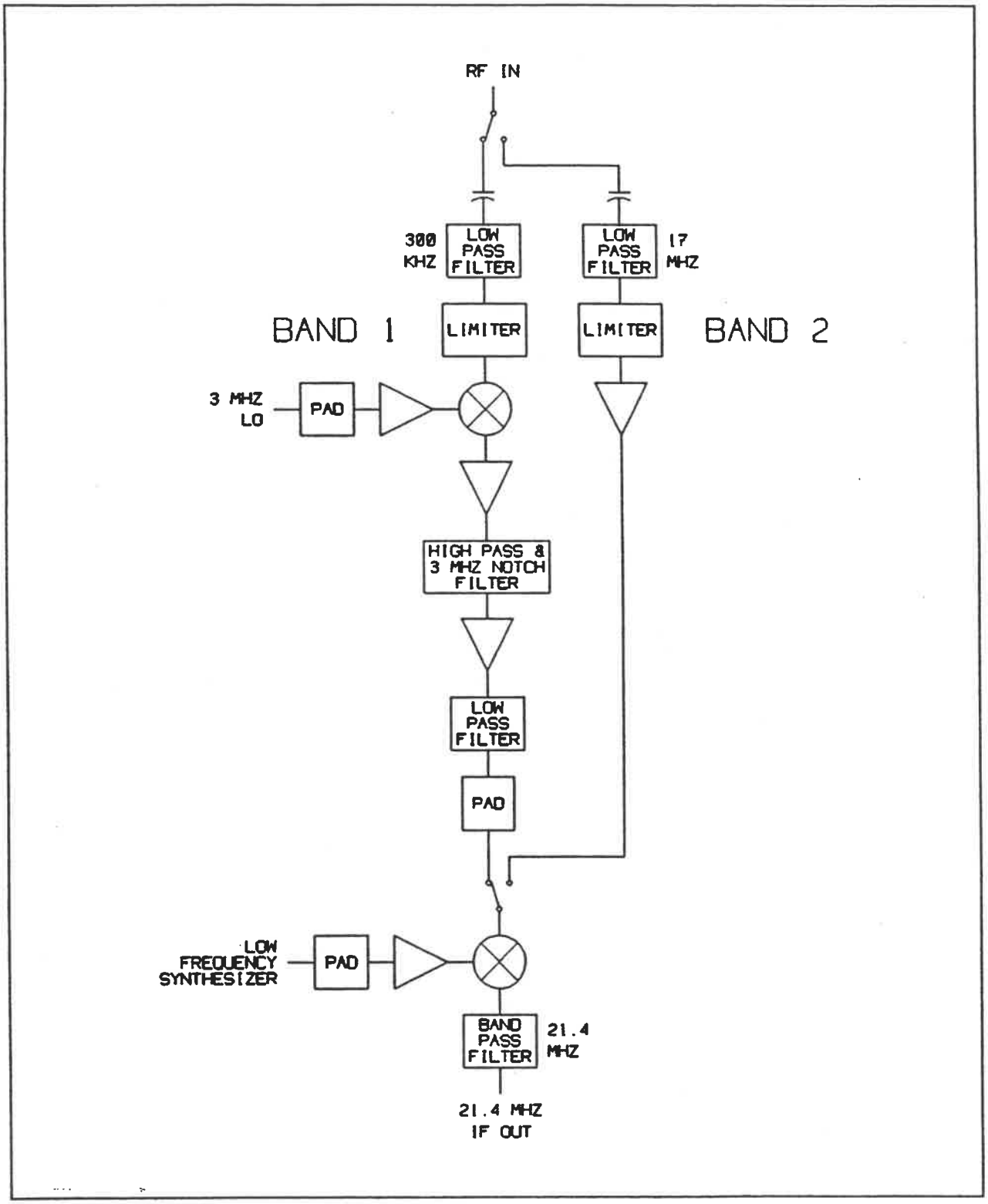

Figure 4-6: Low Frequency RF Module Block Diagram

The output of the mixer feeds a grounded-gate FET amplifer (Q2) which features 6 dB of gain and a low noise figure. The output of this amplifier is transformer-coupled (T1) to a bipolar amplifier (U3) which in turn drives a 3 MHz crystal notch filter circuit which is used to suppress the local oscillator frequency component coming from the mixer. The amplifier's 80 Ohm output impedance is transformed to 3 kOhms at the crystal and back to 35 Ohms at the input to the following amplifier (U6). The higher impedance at the crystal permits a deeper notch at the 3 MHz LO frequency. The amplifier following the crystal drives a lowpass filter (C54 - C59, L21, L22) which passes 3.001 MHz to 3.25 MHz, but attenuates higher frequency components from the mixer. The output signal at this point is not IF yet; it is merely the band 1 input range, up-converted.

The signal then goes through a 10 dB pad (R18 - R20) to a GaAs FET switch (U9) which performs selection between the band 1 and band 2 processing channels. The two signal paths are merged at this point. The GaAs FET switch feeds one input of another double-balanced mixer (U8). The second input of this mixer is driven by a tuneable local oscillator signal which arrives on the module at +2 dBm via a coax connector (J3), and is then stepped up to +7 dBm by an amplifier (U7). In band 1 this LO, provided by the low frequency synthesizer, can range from 24.401 to 24.65 MHz. The output of the mixer feeds a 21.4 MHz bandpass filter (C65 - C69, L24 - L26) which suppresses everything but the difference signal, thus producing a 21.4 MHz IF signal. This signal exits the module via a coax connector (J4). From there the signal goes to the 21.4 MHz IF amplifier module.

Band 2 receives its 250 kHz - 15 MHz signals from the same relay as band 1 (K1), and passes the signal through a DC-blocking capacitor (C4) and 17 MHz lowpass filter (C15 - C22, C25 - C28, C31, C32, L1 - L6) which attenuates out of band signals , LO re-radiation, and image frequencies. The signal then passes through a limiter (CR5, CR6) for protection against transient spikes. The limited output from the lowpass filter then feeds another input of the same GaAs FET switch (U9) that selects the band 1 signal. From this point on the circuitry is shared, the only difference being that in band 2 the tuneable LO can range from 21.65 MHz to 36.4 MHz to provide the fixed 21.4 MHz IF.

Remaining circuitry on the module consists of a transistor switch (Q1) to drive the relay (K1), and a logic-level converter (U1) to drive the GaAs FET switch (U9). Both of these circuits are driven by the same logic signal, sourced at the 21.4 MHz IF amplifier module (A1A6) and carried on a trace across the cardcage backplane.

4.2.3 Microwave RF Module (A1A1)

When tuning in band 3, the signal from the front panel RF section is passed to the preselector module (A1A2), where it is passed through a lumped-element, 1100 MHz low-pass filter (A1A2 FL1). The filtered signal is then passed to the microwave RF module. (This one filter is why A1A2 is called the "preselector module". All of the other circuitry in the module is part of the synthesizer section.) The rest of the circuitry for band 3 processing is contained in the microwave RF module. Figure 4-7 is a block diagram of the processing.

The circuitry begins with the input limiter subassembly (A1A1A1). This consists of a set of diodes (A1A1A1 CR1 - CR4) and a tuned length of 50 Ohm line (A1A1A1 W1). In normal operation the tuned line is inductive, forming a low-pass filter with the capacitance of the diodes. The corner of this filter is at about 1200 MHz. When the input signal exceeds about 300 mV, either positive or negative, the diodes begin to conduct, thus limiting the output from the subassembly by shunting the excess to ground. The capacitance of the diodes changes as they begin to conduct, so that the filter properties of the circuit are corrupted when in limit. Trimming capacitors (A1A1A1 C3, C4) are provided to optimize the VSWR.

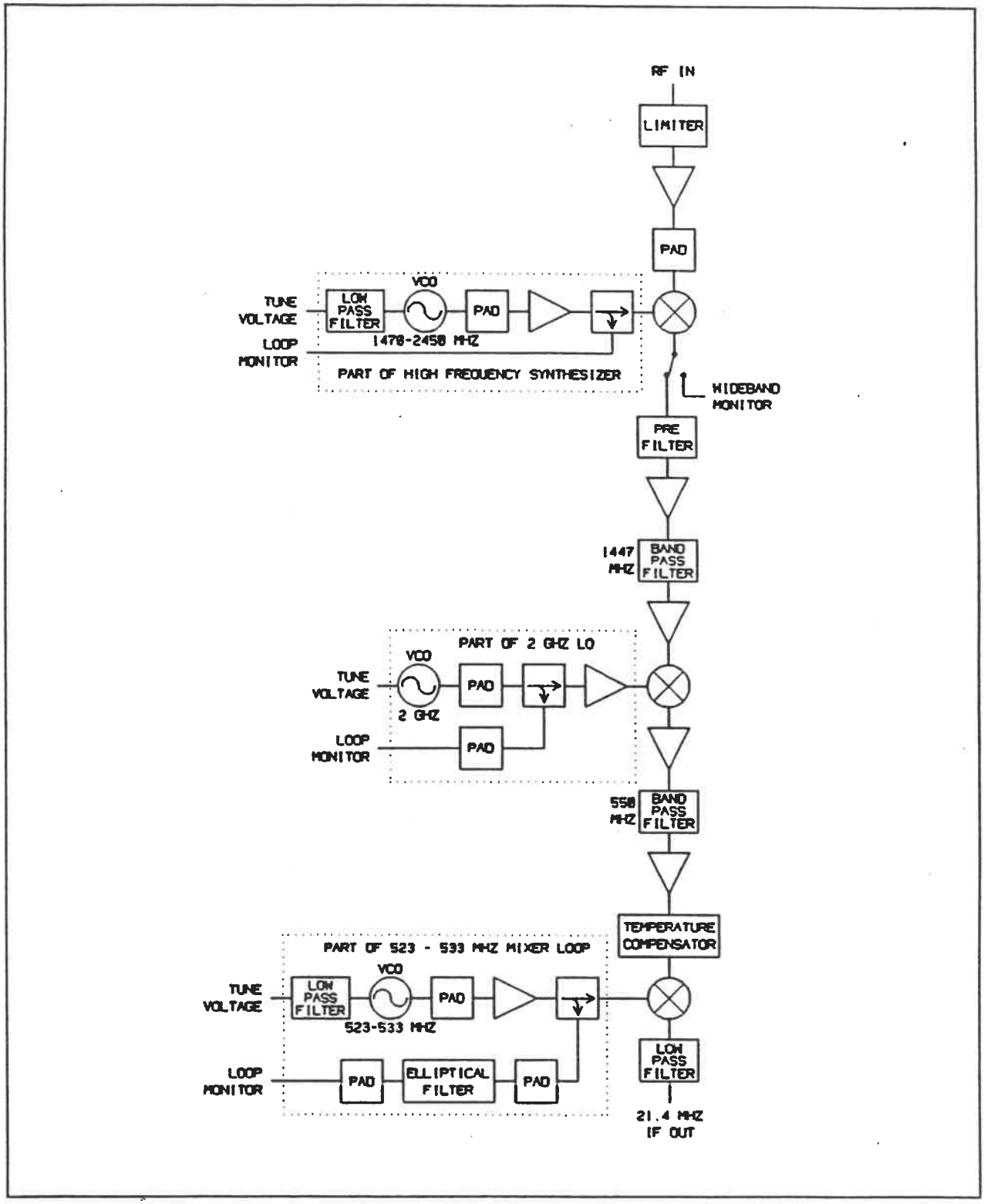

Figure 4-7: Microwave RF Module Block Diagram

The output of the limiter subassembly feeds the first conversion subassembly (A1A1A2). This begins with the RF amplifier (A1A1A2 U1), which provides 14.5 dB of gain and is the major contributor to the noise figure of the radio. The amplifier is followed by a 1 dB pad (A1A1A2 R1 - R3) which is provided to clean up the VSWR of the input of the amplifier, because this component partially reflects its output conditions at its input. The padded signal feeds the first conversion mixer (A1A1A2 U2), the other input of which is the 1470 - 2450 MHz programmable synthesizer output, arriving at approximately +9 dBm. See paragraph 4.6.2 for a description of this LO.

The mixer converts the input to about 1450 MHz. The output of the mixer feeds a GaAs FET switch (A1A1A2 K1) which diverts the signal to wideband output connector (J4) on top of the module when external wideband mode is enabled. The switch requires logic levels of 0 and -8 Volts, in complementary phases, delivered by a translator (U1) from a select signal supplied across the cardcage backplane (A1A20) from the 21.4 MHz IF amplifier module (A1A6).

If not diverted to the wideband monitor jack, the signal is passed to the prefilter/amplifier subassembly (A1A1A3). Here it feeds a 1450 MHz bandpass filter consisting of a pair of adjustable capacitors (A1A1A3 C1, C3) and a length of 50 Ohm line tuned to act as an inductor (A1A1A3 W1), all connected in series. This attenuates the undesired mixing components, and also pads the desired signal by about 1 dB. The filter is followed by an amplifier (A1A1A3 U1) which provides about 9 dB of gain. All of this between the input amplifier and the first conversion amplifier introduce losses of about 10 dB. So while the input amplifier adds 14.5 dB of margin, most of it is used up in the first conversion and filtering, and so components later in the signal path can still have a small effect on the noise figure.

The first conversion amplifier output feeds the second conversion subassembly (A1A1A4). Here it passes through a helical filter (A1A1A4 FL1) which features a center frequency of 1447.5 MHz and a 3 dB bandwidth of 24 MHz. This rejects everything but the desired IF. The filter is followed by an amplifier (A1A1A4 U1) which provides about 9 dB of gain. The amplifier drives the second conversion mixer (A1A1A4 U2), the other input of which is the 2 GHz fixed LO at approximately +9 dBm. See paragraph 4.6.2 for a description of this LO. The result of the conversion is the second IF, ranging around 550 MHz. The output of the mixer feeds the second conversion amplifier (A1A1A4 U3) which provided 12 dB of gain.

The second conversion amplifier output feeds a 550 MHz, lumped-element bandpass filter (A1A1A5 FL1) which rejects everything but the 550 MHz IF. The output of the filter feeds the third conversion subassembly (A1A1A6), beginning with an amplifier (A1A1A6 U5) which provides 12 dB of gain. Following the amplifier is the temperature compensator. Two current sources are connected in series, one temperature-varying (A1A1A6 U8), the other stable (A1A1A6 Q2). At room temperature they pass exactly the same current (about 100 uA), with a trimmer (A1A1A6 R15) provided to balance them. The difference between them therefore varies with temperature. This difference is amplified (A1A1A6 U7) and converted to a voltage. This voltage is then used to control a current source (A1A1A6 Q4) with temperature compensation (A1A1A6 CR5). The current source drives a variable attenuator circuit consisting of PIN diodes (A1A1A6 CR1, CR2) and a tuned length of 50 Ohm line (A1A1A6 W1). The diodes form the legs of a pi-network, and the tuned line forms the bridge. Varying the current source with temperature causes the impedance of the diodes to change, which causes the padding effect of the pi-network to change. The range of adjustment is about 6 dB, with 3 dB applied at room temperature. A trimmer (A1A1A6 R29) is provided to adjust the gain factor of the current source. The temperature compensating circuit uses -8 VDC from the cardcage backplane and +9 VDC developed locally from +15 VDC by means of a regulator (A1A1A6 U6). An enabling switch for the -8 VDC to the circuit (A1A1A6 Q1, Q3) is used to remove the -8 VDC supply from the temperature control circuit should the +15 Volt supply fail.

Once the signal has passed through the temperature compensator it feeds the third conversion mixer (A1A1A6 U4), the other input of which is the 523.6 - 533.6 MHz LO at approximately +9 dBm. See paragraph 4.6.3 for a description of this LO. The result of this conversion is the 21.4 MHz IF, now tuned to the exact center frequency desired. The output of the mixer passes through a 39 MHz low-pass filter (A1A1A6 L5, C18, C19) and is then delivered to the 21.4 MHz IF amplifier module (A1A6).

4.3 21.4 MHz IF Section

The 21.4 MHz IF section consists of two modules: the 21.4 MHz IF amplifier module (A1A6) and the 21.4 MHz IF filter module (A1A8). Signals pass from the outputs of the microwave RF module (A1A1) and the low frequency RF module (A1A5) to the signal inputs of the 21.4 MHz IF amplifier module. After initial selection switching, fixed and variable gain, and overload detection, the signal passes to the 21.4 MHz IF filter module. There the signal passes through one or more bandpass filters, also with switch selection, and more overload detection. The output goes to three destinations: to the video module (A1A9) log detector; to the DCIF module (A1A11) for for narrower bandwidths in log mode; and back to the 21.4 MHz IF amplifier module for further fixed and variable gain, for use with linear mode video. The outputs from this part of the 21.4 MHz IF amplifier module drive the DCIF module, the linear detector in the video module, and the 21.4 MHz IF monitor jack on the rear panel of the receiver.

Note that since the linear mode DCIF pickoff is placed before the end-to-end gain setting circuit, this function must also be supplied in the DCIF. Also, since the log mode pickoffs for both DCIF and wider-bandwidth modes are placed before the last gain-setting circuit, the controllable gain range in log mode is only 2/3 of what it is in linear mode, 33.3 dB vs. 50 dB.

The two 21.4 MHz IF modules will be discussed separately in the following paragraphs. A block diagram of the 21.4 MHz IF section is shown in figure 4-8.

4.3.1 21.4 MHz IF Amplifier Module (A1A6)

The signal path begins with a GaAs FET switch (U10) which selects the module signal input from the outputs of either the microwave RF module (A1A1) or the low frequency RF module (A1A5). The output of the switch is transformer-coupled (T2) to an amplifier (U11) to provide impedance matching. Both signals arrive at 21.4 MHz center frequency and with unwanted mixing products removed. The output of the first amplifier goes in three directions: to the front end overload/underload detector circuit, and then through a splitter (U8) out of the module to the signal monitor jack on the rear panel of the radio; and also to the first of the variable attenuator circuits.

The detector circuit provides a transistor (Q1) amplifier to bring up the signal level without worrying too much about cleanness, followed by a diode detector (CR18), followed by comparators for overload (U20) and underload (U21). The detector output is biased DC positive, and increasing signal levels cause the output to be pulled more negative. For the overload detector a positive threshold is set by a trimmer (R64), lower than the DC bias of the detector output. When the incoming signal level pulls the detector output below the threshold comparison level set by the trimmer, an overload is detected. The trimmer is set so that this happens at -19 dBm signal level entering the module. Similarly, the underload detector has a second positive threshold set by a trimmer (R69). The underload comparator is connected oppositely, so that when the incoming signal level *doesn't* pull the output of the detector below the comparison value set by the trimmer, an underload is detected. The threshold here is set at -32 dBm at the module inputs. Overload and underload status is passed to the cardcage backplane interface circuit for further processing.

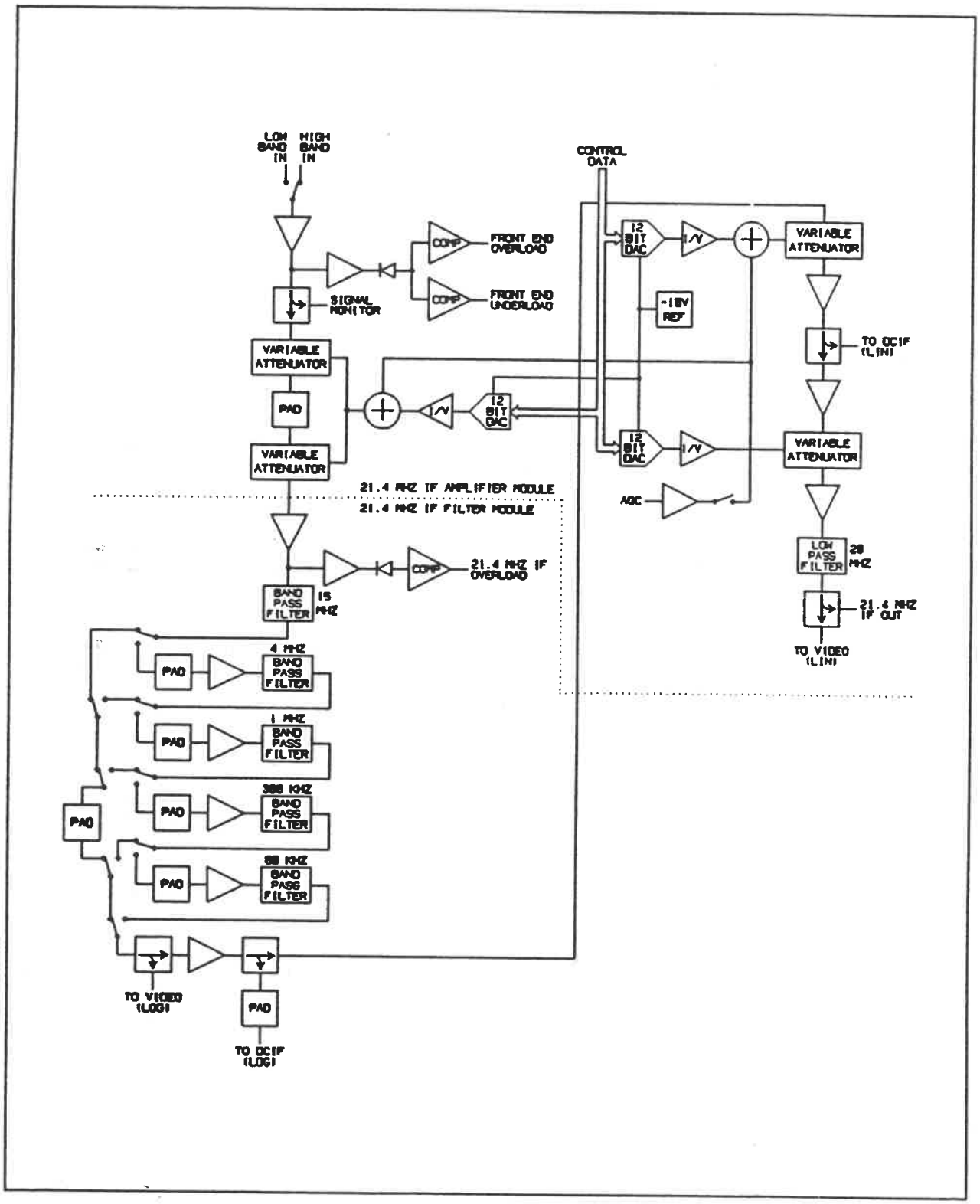

Figure 4-8: 21.4 MHz IF Section Block Diagram

There are four variable attenuator circuits in the module, all identical in implementation but different in how they are controlled. Each has a controllable range of approximately 20 dB. The first two are placed in tandem after the signal monitor output pickoff, with a pad (R35 - R37) between them.

Each attenuator circuit is based on a pair of PIN diodes (CR13, CR14 in the first circuit). These components can vary their impedance of a high-frequency signal based on their DC bias. The signal level must be small for the effect to be linear. The circuitry surrounding the PIN diodes is provided to AC-couple the signal through the diodes, to supply the DC bias and its variation to the proper points, and to block the signal from entering the bias circuits. One diode (CR14 in the first circuit) acts as a coupling diode, for which increased bias will increase signal coupling. The other diode (CR13 in the first circuit) acts as a signal shunt to ground, so increased bias here will decrease the signal level at the output.

Attenuator bias is partly fixed and partly variable. The variable part is controlled partly by AGC (when enabled) and partly by the microprocessor controlling the radio, via DACs. AGC is developed in the video module (A1A9) and is delivered to the 21.4 MHz IF amplifier module as a slowly varying DC level. Entering the module it is amplified (U28) with offset adjusted via a trimmer (R100). This trimmer sets the AGC turn-on point. The output of the amplifier is clamped (CR28) and rectified (CR29) to positive values. A relay (K1) controlled by the cardcage backplane interface circuit acts as an AGC on/off function by connecting/disconnecting the AGC signal to the attenuator circuits. Another trimmer (R101) is provided after the relay to set the off-state contribution.

The first two attenuator circuits are driven by the AGC signal (when selected) and also by the output of one of the control DACs, called DAC A (one of the two separate outputs of U17, converted to voltage output by U12). The DAC output is 0 to +10 VDC. It is reduced via a resistive divider (R87, R88) and then precision rectified (U27, CR25), and then combined with the AGC signal and amplified (U27 again). This output is delivered to the attenuators. The effective voltage range for the attenuator circuits is about +2 to +10 Volts.

The output from the two tandem attenuator circuits is passed to the 21.4 MHz IF filter module where the signal is reduced to 15 MHz bandwidth or less. Returning from the 21.4 MHz IF filter module, the signal passes through the third attenuator circuit. This circuit is controlled by both the AGC voltage used to control the first two attenuator circuits, and also by the output of a second DAC, called DAC B (the other output of U17, converted to voltage output by another section of U12). The DAC output is reduced by a resistor pair (R79, R80), precision rectified (U26, CR23), and combined with the AGC signal and amplified (U26 again) to drive the attenuator circuit.

The output of the third attenuator circuit is amplified (U6), and the linear mode input for the DCIF module is picked off via a splitter (U7). The signal path then continues with another amplifier (U5), followed by the fourth attenuator circuit. This attenuator is provided for end-to-end (predetection) gain setting and is controlled by a DAC only, without contribution from the AGC. The DAC, called DAC C (one of the outputs of U16, converted to voltage output by a section of U12) drives the attenuator circuit directly. The output of the attenuator circuit is transformer-coupled (T1) to an amplifier (U3), through a noise filter (L2, L3, C5, C6, C9) to another amplifier (U2), and is finally sent to the linear detector on the video module, and to the 21.4 MHz IF output jack on the rear panel of the receiver, via a splitter (U1). The noise filter is a low-pass with its cutoff set at 30 MHz. This reduces out-of-band noise contributions from the circuitry located behind the bandpass filters.

A temperature compensation circuit is provided (based on U29 - U31, Q3, Q4, CR30 - CR32), but it is currently unused. If a wider operating temperature range is specified, then it may be placed in service.

The cardcage backplane interface circuit consists of buffering and latching for bus data bits, address decoding, level shifting, and DAC control. A status return circuit for overload and underload are also provided. A precision -10 VDC reference for the DACs (U4) is also provided.

Incoming data is buffered (U15) and passed to a latch (U14). Three of the latch bits are used directly, to enable band selection and AGC. Four more bits are decoded (U13) to form the bandwidth selects. Bus addresses are decoded (U18, U19) to control the data latch and the two DAC ICs (U16, U17). They feature two 12 bit DACs per package, mapped onto the 8 bit data bus. Here is the addressing for the module:

Address 50(hex) - 53(hex) = DAC IC #1 (U17):
- Address 50(hex) = DAC A LSDs:
  - Bits 0 - 7 = DAC A bits 0 - 7
- Address 51(hex) = DAC A MSD:
  - Bits 0 - 3 = DAC A bits 8 - 11
  - Bits 4 - 7 = (unused)
- Address 52(hex) = DAC B LSDs:
  - Bits 0 - 7 = DAC B bits 0 - 7
- Address 53(hex) = DAC B MSD:
  - Bits 0 - 3 = DAC B bits 8 - 11
  - Bits 4 - 7 = (unused)

Address 54(hex) - 57(hex) = DAC IC #2 (U16):
- Address 54(hex) = DAC C LSDs:
  - Bits 0 - 7 = DAC C bits 0 - 7
- Address 55(hex) = DAC C MSD:
  - Bits 0 - 3 = DAC C bits 8 - 11
  - Bits 4 - 7 = (unused)
- Address 56(hex) = DAC D LSDs:
  - Bits 0 - 7 = DAC D bits 0 - 7
- Address 57(hex) = DAC D MSD:
  - Bits 0 - 3 = DAC D bits 8 - 11
  - Bits 4 - 7 = (unused)

Note: DAC D is currently unused.

Address 58(hex) = load all DACs strobe (data unimportant)

Address 59(hex) = data latch:
- Bits 0 - 2 = bandwidth code:
  - 000 = 15 MHz*
  - 001 = (reserved for 8 MHz*)
  - 010 = 4 MHz*
  - 011 = 1 MHz*
  - 100 = 300 kHz*
  - 101 = 80 kHz*
  - 110 = (unused)
  - 111 = wideband*
- Bit 3 = bandwidth enable:
  - 0 = disable
  - 1 = enable
- Bit 4 = high/low band select:
  - 0 = high band (band 3)
  - 1 = low band (band 1/2)
- Bit 5 = band 1/band 2 select:
  - 0 = band 2
  - 1 = band 1
- Bit 6 = AGC enable:
  - 0 = disable
  - 1 = enable
- Bit 7 = (unused)

The bandwidth select lines are routed through the cardcage backplane to the 21.4 MHz IF filter module. The band 1/band 2, high/low band, and wideband select lines are also routed onto the cardcage backplane, for use by the microwave RF module and the low frequency RF module. The high/low band select line also drives a level shifter (U9) which provides the 0 and -8 Volt logic levels required by the GaAs FET switch on the module input.

The status return circuit takes its inputs from the front end overload and underload detection comparators. The underload input drives a retriggerable monostable multivibrator (U25) and recombination gate (U24) which ensures that underload must be present for at least 200 uS before underload status is placed on the bus. The backplane trace (B20) is driven through a tristate driver (U22). Meanwhile, the overload input is stretched and filtered (U22, CR22, C93), and drives both the backplane combined front end overload (B21) and the discrete 21.4 MHz IF front end overload (A17) traces through tristate drivers (U22). Currently the combined front end overload line is only driven by this circuit.

4.3.2 21.4 MHz IF Filter Module (A1A8)

This module takes its input from the 21.4 MHz IF amplifier module (A1A6) and provides outputs to the video module (A1A9) log input, the DCIF module (A1A11), and back to the 21.4 MHz IF amplifier module. Bandwidth selection control is taken from the cardcage backplane, supplied by the IF amplifier module, and back end overload detection outputs are placed the cardcage backplane as well.

The signal path begins by transformer-coupling (T1) the signal from the IF amplifier module to an amplifier (U1) which adds 14 dB of gain. The amplifier output is sampled by the back end overload detection circuit and is transformer-coupled (T2) to drive the 15 MHz bandpass filter. The overload detector consists of a transistor amplifier (Q1) followed by a diode detector (CR2) and storage capacitors (C12, C13). the detector output is sampled by a comparator, using a positive DC reference set by a trimmer (R1) as a threshold. The signal pulls a positive DC bias in the detector output downward, so that a signal in excess of -34 dBm at the module input pulls will pull the detector output below the comparator threshold, triggering an overload status condition. The comparator output is stretched and filtered (U3, CR3, C23) so that an impulsive overload will provide about a 1 uS status pulse. The filtered output is delivered to the cardcage backplane combined back-end overload line (A20) and the 21.4 MHz IF overload line (B18) via tristate drivers (U3).

The 15 MHz bandpass filter consists of an LC network (L7 - L9, C6, C7, C30 - C32). Its output feeds a GaAs FET switch (U6) which directs the signal either to the input or the output of the 4 MHz bandpass filter.

The 4 MHz filter begins with a 5 dB pad (R33 - R35) followed by an amplifier (U5) which adds 14 dB of gain, for a net gain of 9 dB. The amplifier is followed by an RLC network (L10 - L15, C36, C38, C40, C42, C43, C45, C47, C49, R19 - R21, R23 - R26) which establishes the filter characteristic. The network is followed by a GaAs FET switch (U9) which directs the output of the filter either to the input of the 1 MHz bandpass filter or to another GaAs FET switch (U22) which selects either the outputs of the 4 MHz filter or the 15 MHz filter for output from the overall filter section.

The 1 MHz bandpass filter begins with a 6 dB pad (R42 - R44) followed by an amplifier (U8) providing 14 dB of gain, for a net gain of 8 dB. The amplifier is followed by an LC network (L19 - L23, C54 - C72, C100), followed by a GaAs FET switch (U12) which directs the output of the filter either to the input of the 300 kHz bandpass filter or to another GaAs FET switch (U23) which selects either the output of the 1 MHz filter or the signal selected from the outputs of the 4 MHz and 15 MHz filters for output from the overall filter section.

The 300 kHz bandpass filter begins with a 2 dB pad (R56 - R58) followed by an amplifier (U11) providing 14 dB of gain, for a net gain of 12 dB. The amplifier is followed by an LC network (L26 - L29, C75 - C86, C105), followed by a GaAs FET switch (U15) which directs the output of the filter either to the input of the 80 kHz bandpass filter or to another GaAs FET switch (U24) which selects either the output of the 300 kHz filter or the signal selected from the outputs of the 1 MHz, 4 MHz, and 15 MHz filters, padded by 4 dB (R47, R48, R59), for output from the overall filter section.

The 80 kHz bandpass filter begins with a 7 dB pad (R67 - R69) followed by an amplifier (U14) providing 14 dB of gain, for a net gain of 7 dB. The amplifier is followed by a crystal filter (FL1), which is followed by a GaAs FET switch (U17) which selects either the output of the 80 kHz filter or the signal selected from the outputs of the 300 kHz, 1 MHz, 4 MHz, and 15 MHz filters, for output from the overall filter section.

The idea is that the radio will normally be used for receiving signals which are mostly impulsive, which means that signal level is directly proportional to bandwidth. Noise in band, however, is proportional to the square root of the bandwidth. Amplification has therefore been provided in each bandwidth filter which will normalize the noise, that is, the amplification factor is proportional to the square root of the reduction in bandwidth. For example, since the reduction in bandwidth between the 1 MHz filter and the 4 MHz filter is a factor of four, the 1 MHz filter section requires an overall extra gain of the square root of four, or two. In actuality, a 14 dB amplifier and a 6 dB pad are provided, with the odd 2 dB being absorbed by the passive filter components, switches, etc.

The bandwidth filters are Chebyshev type, with a 60 dB bandwidth approximately four times the 6 dB bandwidth. The switching is set up so that for any given bandwidth the signal must pass through the associated bandwidth filter and all wider ones as well, in sequence. In other words, for 300 kHz bandwidth, the signal passes through the 15 MHz filter, followed by the 4 MHz filter, followed by the 1 MHz filter, followed by the 300 kHz filter, with only the 80 kHz filter omitted. By doing this the gain is gradually increased as the bandwidth is gradually reduced, which yields the best dynamic range.

The output from the final selection switch drives a splitter (U18). One output of the splitter is routed to the log input on the video module through a pad (R78 - R80) for use in non-DCIF log mode. The other splitter output is transformer-coupled (T3) to an amplifier (U20) which provides 14 dB of gain. The amplifier drives another splitter (U19), one output of which is returned to the IF amplifier module at +10 dBm full scale. The other splitter output is routed to the log mode input of the DCIF module through an 8 dB pad (R81 - R84) at +2 dBm full scale.

The remaining cardcage backplane interface consists of level translators for the filter select lines provided by the 21.4 MHz IF amplifier module. The GaAs FET switches require logic levels of 0 and -8 Volts in complementary phases, which are provided by comparators acting as level shifters from the incoming TTL (U4, U7, U10, U13, U16). Incoming select signals are valid when low. Switching is set up so that a given filter output is routed to the module outputs when selected, or to the input of the next narrower filter stage when not selected. The 15 MHz filter is always in the signal path, one way or another.

4.4 DCIF Module (A1A11)

The DCIF module (A1A11) begins with a signal taken from the 21.4 MHz IF, provides programmable bandwidths from 200 Hz to 20 kHz, provides programmable back-end gain, and provides AM detection for its available bandwidths, producing an output which is sent to the video module. Note that the DCIF is only in use when one of its bandwidths is selected, and is completely bypassed and shut down otherwise.

The module consists of the following circuits:

- input section, consisting of an LO amplifier, quadrature splitter, and carrier elimination (envelope) filters
- gain recovery amplifiers for each phase
- programmable switched-capacitor filters for each phase
- multiplying DACs for each phase
- precision rectifiers for each phase
- a square-root-of-the-sum-of-the-squares circuit
- a programmable timebase with multiple outputs
- an overload detection circuit
- a logic and control circuit

These circuits perform the following receiver functions:

- narrow bandwidth filtering from 200 Hz to 20 kHz
- programmable gain in the back end, for proper gain distribution
- AM detection for narrow bandwidths
- back end overload status for narrow bandwidths

Discussion will proceed from signal input to signal output, with additional descriptions of peripheral circuits provided where appropriate. The block diagram of the section is shown in figure 4-9.

The signal path begins with the input section, which produces two output channels in quadrature. Each channel contains three programmable filters and two programmable amplifiers. Following all of that the channels must be recombined to form the output. The idea behind the DCIF lies in the fact that a signal may be split into two components which always differ in phase by 90 degrees, each phase may be identically processed, and the results recombined in a vector sum, without losing information. In the case of the DCIF, "processing" consists of converting to baseband, bandlimiting, and gain setting. By doing it this way the usual bulky, heavy crystal filters required for each desired bandwidth are eliminated. The drawback is that both phases must be processed *identically*. Identical in gain, in phase, in frequency response, and in DC offset. Any mismatch will produce distortion in the output, normally in the form of "motorboating", in which the beat frequency between the tuned signal from the 21.4 MHz IF and the 21.4 MHz LO, produced by the mixer/splitter, is imperfectly cancelled when the two channels are recombined. In order to minimize this problem a number of corrective factors and adjustments have been provided in the DCIF. These will be detailed as part of the following descriptions as well.

The input section is based on a quadrature mixer/splitter (U11) which mixes the input from the 21.4 MHz IF section with a fixed 21.4 MHz IF LO signal from the synthesizer section, thus converting the signal to baseband. The LO arrives on the module at -10 dBm and is amplified by an op-amp (U10) to +16 dBm. Through the source resistor, it drives the mixer/splitter at +10 dBm. The LO is transferred at a low level in order to minimize pickup by other modules. The signal input may be taken from either of two points in the 21.4 MHz IF, depending upon whether or not log compression is selected in the video section. Different inputs are required for the gain distribution to come out right. Input selection is performed by a relay (K1), set by the logic and control circuit. Of the four programmable gain stages in the 21.4 MHz IF, the tap for the DCIF in linear mode precedes the last one (which is responsible for setting end-to-end gain for the radio) and the tap for the DCIF in log mode precedes the last two, which cuts into the IF gain control range. In each case the correction must be made up in the DCIF's programmable gain stages. In practice, the linear tap sees up to 18 dB more gain from the 21.4 MHz IF than the log tap, but a full-scale signal at each input is -6 dBm. The selected signal drives the mixer/splitter directly.

The mixer/splitter has two outputs which differ in phase by 90 degrees, one called "in-phase" and the other "quadrature" (I and Q). Each output passes through a two-pole low-pass L-C filter to remove everything but the difference component from the signal. The bandwidth of the signal from the 21.4 MHz IF is always limited to 80 kHz, and the widest bandwidth expected from the DCIF is only 20 kHz, so a two-pole filter with its corner at 700 kHz is sufficient to get rid everything but the baseband signal. Components are selected during module test for the best match between channels. A trimmer (C33) is provided to adjust the mixer/splitter to exactly 90 degrees of phase shift between the outputs.

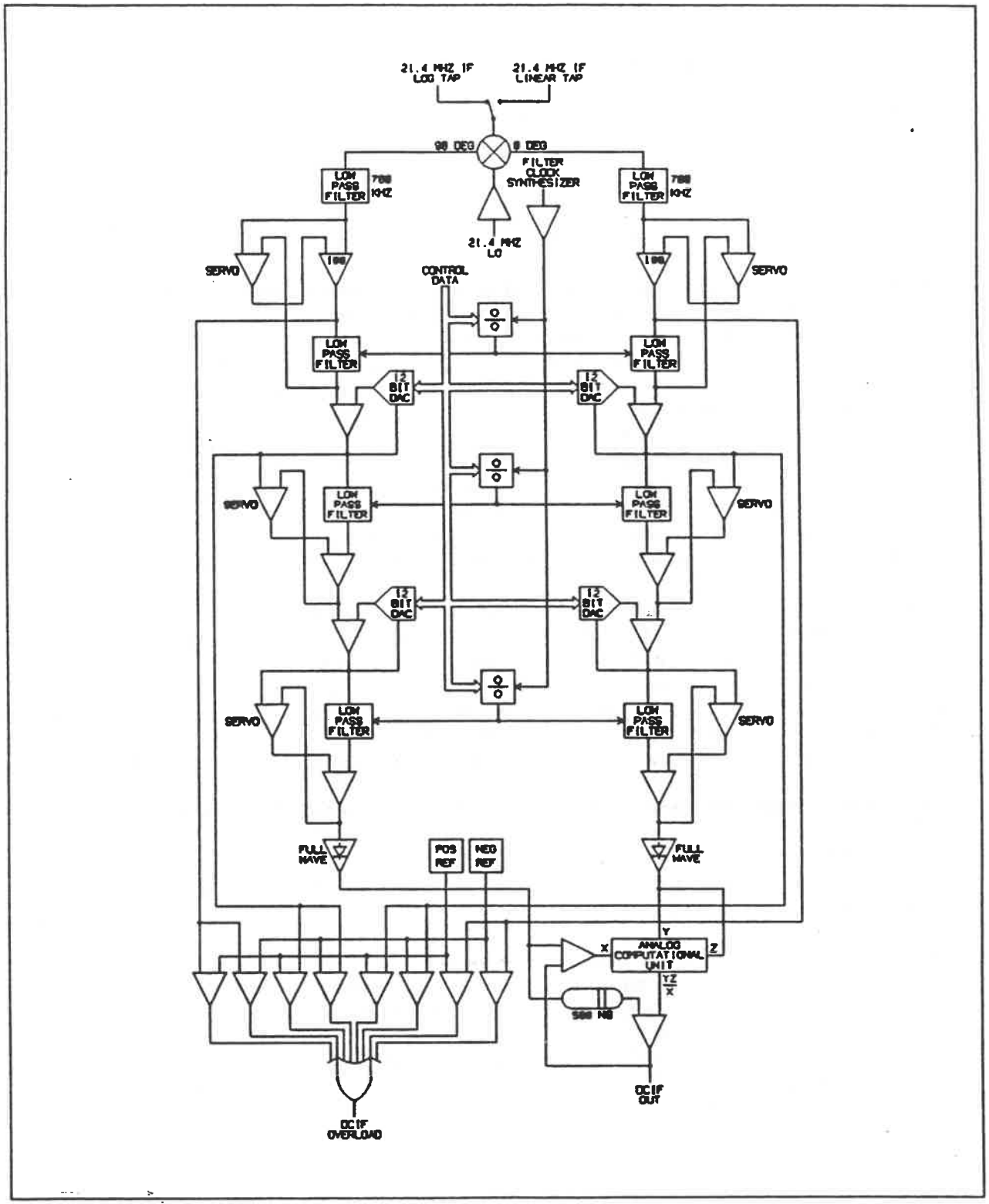

Figure 4-9: DCIF Block Diagram

After the filters, the outputs from the mixer/splitter are at at 50 mV peak, full-scale, so each output is provided with a 40 dB fixed-gain low-noise amplifier (U14 and U13). Full-scale outputs from these amplifiers are 5 Volts peak, and are clamped to +/- 7 Volts by diodes (CR3 - CR8), to prevent both turn-on transients and disabled-state servo drift from damaging the circuits which follow, which use smaller power supply voltages. The amplifiers also provide a pole of high-end rolloff with the corner at about 25 kHz, for noise filtering. The rolloff capacitors (C36, C42) and the timing capacitors in the servo amps (C28, C29) are matched in pairs before production. The servo gain-setting resistors (R34, R35, R39, R40) are selected during module test for the best match between channels. Servo gain must be set to match the gain of the signal amplifiers as well.

The gain-recovery amplifiers are followed by the first bandwidth filters. Each amplifier/filter combination is provided with a chopper-stabilized servo amplifier (U12) to eliminate any long-term DC components, since any offset will easily saturate the module output at narrow bandwidths (where bandwidth-compensating gain is highest). The overall structure at this point, in each channel, consists of a programmable filter, followed by a programmable gain unit, followed by another programmable filter, followed by another programmable gain unit, followed by another programmable filter. Although a single filter provides adequately sharp cutoff at the edge of the passband, a second filter is necessary in front to prevent aliasing around the filter clock, and a third filter is necessary in back to make sure that the clock of the second filter doesn't appear in the output at smaller bandwidths. A discussion of how the filters work will shed more light on this.

The filter ICs (U15, U16, U19, U20, U25, and U26) are switched-capacitor low-pass types with eight poles apiece. The middle one in each chain of three (U19, U20) sets the overall bandwidth and is a Bessel type (linear phase), selected to minimize impulsive overshoot. The other two are Butterworth types, selected to provide rapid rolloff without too much phase nonlinearity. The cutoff frequency of each filter is determined by the frequency of an applied clock signal, and by a select line which determines whether the cutoff will by 1/75 or 1/150 of the clock frequency for the Bessel filter, or 1/50 or 1/100 of the clock frequency for the Butterworth filters. Gain through the filters inside the passband is near unity, though with a bit of DC offset. Dynamic range is about 60 dB for a full-scale input of +/- 5 Volts. Offset of the second and third pairs of filters is nulled by servo amplifiers (U22, U28) in conjunction with unity-gain signal amplifiers (U21, U27). The servo timing capacitors (C77, C90, C97, C99) are matched before production.

The filter works by sampling the input at the applied clock rate and then processing it. This means that there is a Nyquist point at half the clock rate, above which any signal present at the input will begin to reflect at the output down inside the passband. It is therefore necessary to band-limit the input of each filter so that there is no signal component above half the clock frequency with an amplitude greater than 60 dB below full scale. Furthermore, the clock frequency will appear in the output and must also be filtered out.

Incoming bandwidth is 80 kHz from the 21.4 MHz IF. In the worst case, the selected bandwidth is 200 Hz, which, since we're now at baseband, requires a low-pass filter with a cutoff at 100 Hz. For the middle filter, assuming that a 150:1 ratio has been selected, the required clock rate is 15 kHz. The Nyquist frequency is therefore 7.5 kHz, and we need to be sure that there is no signal going into the filter at or above this frequency. That is what the pre-filter does. It's own Nyquist frequency is well above the incoming bandwidth.

Meanwhile, the output from the middle filter will contain clock products at 15 kHz, which while outside the maximum passband of 10 kHz is still low enough to cause trouble at the recombination stage. A post-filter is provided to take care of the situation. Clock products from the post filter are too high in frequency to bother the recombination circuitry. Note too that clock products from the pre-filter, at 7.5 MHz or so, are too high to bother the middle filter either.

Three different clock frequencies are therefore required. A timebase with multiple outputs has been provided to accommodate this. This timebase consists of a programmable phase locked loop in the synthesizer section and a programmable counter-timer chip (U2) in the DCIF section. The output from the phase-locked loop ranges from 3 to 9 MHz in 50 kHz steps (but is shut off when the DCIF is not in use) at -10 dBm. When it arrives on the DCIF module it is squared up by a comparator (U1) and clocks the counter-timer chip. The counter-timer chip contains three programmable dividers which can range from division by 1 to division by 65,536. One output is provided for each pair of filter chips, matched up in the I and Q channels. Using various combinations of PLL frequency and divider ratio, many different bandwidths may be programmed.

This takes care of filtering. The channel recombination circuit effectively eliminates residual clock content from the module output for wider passbands.

The other big consideration is gain. The following factors contribute:

- fixed-value gain setting and recovery from the mixer/splitter and filter losses
- variable gain setting due to bypassing the end-to-end gain control in the 21.4 MHz IF
- variable gain setting due to (in log mode) bypassing 1/3 of the gain control range in the 21.4 MHz IF
- variable gain setting for noise level equalization, which varies with selected bandwidth

CW signals passing through the DCIF remain constant in amplitude when they are tuned within the selected bandwidth. Impulsive signals are reduced in the same proportion as the bandwidth. In other words, an impulse coming in at 80 kHz bandwidth will be reduced by 52 dB at a selected bandwidth of 200 Hz. Broadband noise is reduced in proportion to the square root of the reduction in bandwidth, so that noise in a 200 Hz bandwidth is 26 dB less than the noise in an 80 kHz bandwidth. In the R-110, noise at the output is equalized with changing bandwidth by adding gain in proportion to the square root of the change. Thus DCIF requires 20 dB more gain at 200 Hz bandwidth than it does at 20 kHz, with many other values in between.

IF gain control has a range of 50 dB. In log mode the DCIF is expected to provide 1/3 of this range, or about 17 dB. The end-to-end gain control in the 21.4 MHz IF has about the same range, but in practice the necessary variation is considerably smaller, on the order of 5 dB. This must also be available in the DCIF.

The DCIF therefore needs a maximum gain control range of at least 25 dB, and optimally over 30 dB to allow for extreme cases. Fixed gain is also necessary. Since the dynamic range of the programmable filters is marginal for log mode, programmable gain has been provided in two places, once after the pre-filter and once after the main filter. This allows for a two step reduction in bandwidth and a two step recovery of gain, which minimizes degradation in dynamic range by keeping impulsive signals closer to full-scale in amplitude, while gradually reducing the bandwidth.

Gain control is implemented by means of multiplying digital to analog converters (U18 and U23) which multiply an applied signal by a digital code. In this case a pair of dual 12 bit DACs are used, each DAC supplying gain control for matching points in each channel in each of its halves. Output is in current mode, and is converted to voltage mode by op-amps (U17, U24), which are again dual units to best match the channels to one another. Trimmers to null any DC offset (R41, R46, R60, R65) are also provided. The DACs are connected in gain mode rather than attenuation mode, so that the gain for each DAC is set by the formula

$$gain = \frac{4096}{code}$$

As this formula indicates, the granularity of gain control is greatest at when gain magnitude is smallest, and vice versa. It is still within 1% of optimum at the highest gains required, however, and is still closely matched between channels at any setting. While very high gain values are possible using this circuit, they are unnecessary as implemented in the DCIF, and in any case will eventually be slew rate limited by the selected ICs.

Once filtering and gain are taken care of, the two channels must be recombined. Since they are in quadrature, a vector sum is required. Algebraically, this means taking the square root of the sum of the squares. Electrically, the job is performed by an "analog computation unit" IC (U37) and surrounding circuitry. The ACU can't deal with negative-going inputs, so each channel is provided with a precision rectifier circuit. Each circuit begins with a fast op-amp (U29, U34) with diodes in the feedback (CR9 - CR12) to produce two half-waves of precision rectification. Each half-wave is provided with a buffer amplifier (U30, U35), and the results are combined in a final summing amplifier (U31, U36) to produce a full-wave rectified output. DC offsets cause proportional distortion here, and are trimmed out both at the inputs (R84, R106) and at the summing amps (R93, R121). Gains in the half-waves are matched by selecting resistors during module test (R85, R88, R112, R116), and gains between the I and Q channels are matched by a trimmer in the Q channel (R105).

The analog computational unit has three inputs called X, Y, and Z, and one output. The output is equal to YZ/X. A pair of unity-gain summing amplifiers (U32, U38) and a buffered delay (L59, C130, L60, C131, and U33) comprise the rest of the recombination circuit. A trimmer (R100) is provided to compensate the gain in the delay amplifier for losses in the reactive components.

The rectified I channel drives both the Y and Z inputs of the analog computational unit, producing I^2/X. The output of the analog computational unit is summed with the delayed, rectified Q channel output (the delay is provided to match the delay of the ACU, which is about 500 uS). The output of this summing amplifier (U38) is again summed with the rectified output of the Q channel, this time without the delay. The result is fed back to the X input of the ACU. The output of the circuit (and of the DCIF) is taken from the output of the first summing amplifier. Algebraically, we have

$$V_o = \frac{I^2}{V_o + Q} + Q$$

$$V_o(V_o + Q) = I^2 + Q(V_o + Q)$$

$$V_o^2 = I^2 + Q^2$$

$$V_o = \sqrt{I^2 + Q^2}$$

The output therefore provides full-wave envelope detection, and at full scale will produce five Volts peak. Dynamic range is about 60 dB for most bandwidths, and impulsive overshoot is well controlled.

Overload detection is performed in two places in each channel: at the output of the gain recovery amplifier following the mixer/splitter, and at the output of the first programmable gain stage. Separate detectors are provided for signals both too positive-going and too negative-going. The detection circuit consists of comparators (U39, U40) whose outputs are wire-ORed to form a single status line. The threshold for the positive-going detector (U39) is set to +5 Volts, while the threshold for the negative-going detector (U40) is set to -5 Volts. Hysteresis is provided around the comparators, inverted by a transistor (Q2) in the case of the negative detector. The status line feeds the logic and control circuit.

The logic and control circuit handles the interface to the cardcage bus and provides address recognition, control bit latching, and status return for the DCIF. Address recognition is provided by decoders (U5, U6). Data and control lines from the bus are passed through buffers (U3, U9) and are passed to the timebase counter-timer (U2), the gain DACs (U18, U23) (along with some address lines), and to a latch (U4) which stores the discrete control bits. The counter-timer and the DACs have internal data latches.

Here is the address mapping of the DCIF:

Addresses 40(hex) - 43(hex) = counter-timer:
- Address 40 = divider #1 load data
- Address 41 = divider #2 load data
- Address 42 = divider #3 load data
- Address 43 = mode control

Address 44(hex) - 47(hex) = first gain DAC:
- Address 44 = I channel load data (lower 8 bits)
- Address 45 = I channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare
- Address 46 = Q channel load data (lower 8 bits)
- Address 47 = Q channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare

Address 48(hex) - 4B(hex) = second gain DAC:
- Address 48 = I channel load data (lower 8 bits)
- Address 49 = I channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare
- Address 4A = Q channel load data (lower 8 bits)
- Address 4B = Q channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare

Address 4C(hex) = discrete control bit latch:
- Bit 0 = filter #1 and filter #3 ratio select:
  - 0 = 100:1
  - 1 = 50:1
- Bit 1 = filter #2 ratio select:
  - 0 = 150:1
  - 1 = 75:1
- Bit 2 = input select:
  - 0 = linear mode IF tap
  - 1 = log mode IF tap
- Bit 3 = timebase clock and status driver enable:
  - 0 = disable
  - 1 = enable
- Bits 4 - 7 = spare

Address 4D(hex) = DAC load strobe:
- Bits 0 - 7 = spare

Writing to the DACs consists of sending new data to any DAC address which requires it and then writing to the DAC load strobe address, which will cause all four DACs to be updated simultaneously. Data is buffered in the DACs without being actually applied until the strobe is received. Data written to the strobe address is not used -- it is the act of writing which creates the strobe.

A level shifter (U7) is used to convert ratio select bits to the logic levels used by the filter ICs. The input select signal is level shifted and then drives a transistor switch (Q1), which in turn controls the coil of the input select relay (K1). The timebase and status on/off switch acts as an on/off switch for the DCIF: when the DCIF is not in use it is set to "off", and when the DCIF is activated it is set to "on". It disables the timebase by disabling the comparator (U1) which squares up the input from the timebase PLL in the synthesizer section. It disables the status return by disabling the input to the bus status line drivers (U8). These drivers are configured so that their outputs are either tristate (and pulled up by the control circuitry in the front panel assembly) or active low. Two drivers are used by the DCIF: one for the common back-end overload line (STAT2) and one for the DCIF-specific overload line (STAT6).

4.5 Video Module (A1A9)

The video module (A1A9) consists of the following subsections:

- the wideband AM detector
- the log detector
- the BFO (beat frequency oscillator) and its mixer
- the carrier removal (envelope) filter
- the settable noise filter
- the video output amplifier
- the Z axis output amplifier
- the back end video overload detector
- the logic and control section

Using these circuits, the following receiver functions are performed:

- wideband AM detection
- narrowband AM post-processing (detection performed by DCIF)
- wideband log detection and narrowband log-characteristic compression
- BFO detection
- video noise filtering
- video output
- Z axis output
- audio signal source
- DVM signal source
- AGC signal source
- back-end overload detection

The implementation of each of these functions will be described individually. A block diagram of the video module is shown in figure 4-10.

There are three signal inputs to the video module: two from the 21.4 MHz IF and one from the DCIF module. The 21.4 MHz IF is tapped in two different places, once for AM and BFO detection and once for log detection, so that the gain distribution will work out correctly in each case. The requirements for each are different because the log detector has over 60 dB of dynamic range while the linear detector has only a little more than 30 dB. The BFO uses the same input as the AM detector because here the available dynamic range is not a consideration.

The 21.4 MHz IF input destined for wideband AM detection is routed to the detector circuit through a pad (R24 and R25). The value of the pad is selected during module test to place the full-scale input at the threshold of detector overload. While the detector itself is basically a diode (CR1), dynamic range is maximized by placing the diode behind a tuned amplifier which steps the signal level up to a point where the effect of the turn-on characteristic of the diode is minimized. The tuned amplifier is based on a transistor (Q1) and a low-Q tuned network (L6, L7, C26, R33, R34). The diode is followed by an op-amp (U17). The gain of the op-amp is set during module test (by selecting R76 and R77) to establish end-to-end gain. Another diode (CR2) provides temperature compensation and DC offset balance. The detector circuit is followed by the carrier removal filter, an 8-pole low-pass L-C implementation with its corner at 8 MHz. This filter is also used by the log detector.

The output of the filter provides the input for a second, settable video noise filter. This filter is a one-pole low-pass R-C configuration, in which any combination of four capacitors may be selected by the logic and control circuit. In practice only one (or none) is selected at any given time. Which capacitor is selected depends on the radio's selected bandwidth. The corner frequency for each step is shown in table 4-2.

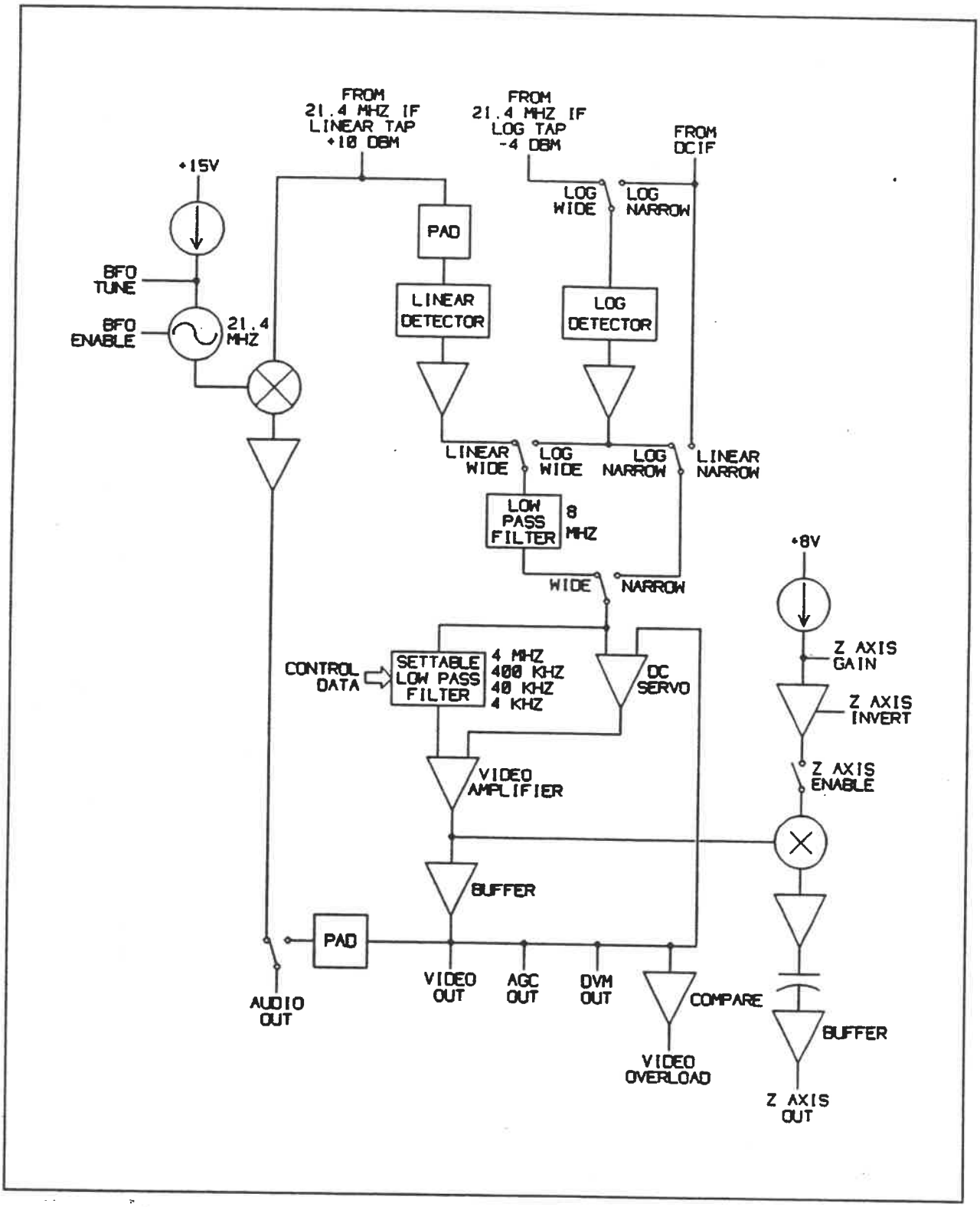

Figure 4-10: Video Module Block Diagram

Table 4-2: Video Noise Filter Selection

Bandwidth Range	Filter Corner
200 Hz - 2 kHz	4 kHz
2.5 kHz - 20 kHz	40 kHz
80 kHz	400 kHz
300 kHz - 1 MHz	4 MHz
4 MHz - 15 MHz	None

The video filter feeds the video output amplifier, which consists of a wideband opamp (U19), followed by a video buffer (U20), and DC-stabilized by a servo amplifier (U18). The servo integrates the difference between the output of the video buffer and the input taken *before* the settable filter, using a very slow time constant. Its output is subtracted from the input taken from the settable filter to eliminate any internal DC offset from the amplifier.

The video buffer is capable of driving multiple 50 Ohm loads, and is used to supply the video, audio, DVM, and AGC outputs, and the detector overload circuit. Of these, only the video and DVM outputs are 50 Ohms, since they are the only ones that need to retain full bandwidth off of the module.

End-to-end gain of the wideband AM detector function is 12 dB, so that a +10 dBm input will produce a full-scale output of 0 to 4 Volts peak. Dynamic range at full scale output is at least 30 dB.

The input for the log detector can come from one of two places, either from the other 21.4 MHz IF input (the one that *doesn't* supply the wideband AM detector) or from the DCIF. Selection is made by a relay driven by the logic and control circuit. A termination resistor is switched onto the 21.4 MHz IF input when it is not in use. Furthermore, the input from the DCIF may be switched around the log detector, bypassing it, when a linear characteristic is desired. When routed through the log detector the DCIF signal, while it arrives already detected and carrier-filtered, is given the same log-compression gain characteristic as the detected signal from the 21.4 MHz IF.

The log detector consists of a pair of log amplifier/detectors (U1 and U2) followed by a linear amplifier (U3) which provides a voltage output. The IF signal from the input is fed in series from the first log amp to the second, while their detected video outputs are summed at the voltage amplifier. An input offset adjustment (R6) is provided to null the output of the log amps. A resistor (R20) is selected during module test to set the full scale output level at the output of the voltage amplifier. The output of this amplifer is fed to the same 8-pole carrier removal filter used by the wideband AM detector, with a relay (K2) performing the selection. From there the signal path is the same as that taken by the wideband AM signal, through the video noise filter and the main video amplifier to the video, audio, DVM, and AGC outputs, and to the Z axis output and detector overload circuits.

Gain is set so that at full scale, every 10 dB coming into the log detector will produce 500 mV at the video output. Dynamic range at full scale is in excess of 70 dB. The RF sections of the log amplifier/detectors have a bandwidth of 120 MHz, while their video outputs have a bandwidth of at least 8 MHz.

The BFO detector consists of a 21.4 MHz Clapp oscillator based on a crystal (Y1) and driven by a transistor (Q4), fine-tuned by a varactor diode (CR3). An on/off switch is provided by a FET switch (U6), which disables the oscillator by removing power from it. Tuning frequency control is provided by a potentiometer on the front panel. A constant current source based on a FET (Q3) drives the front panel control, developing a voltage which varies linearly with its setting while requiring only one "hot" line and a return running off of the module. The voltage derived from the control setting is used to tune the varactor. A trimmer (R112) on the module is used to locate the proper range of tuning adjustment.

The oscillator drives a mixer (U21), the other input of which is the *same* tap of the 21.4 MHz IF used by the wideband AM detector. The difference output generated by the mixer is offset from baseband by an amount determined by the front panel control setting, within a range of +/- 4 kHz. The output of the mixer is filtered to remove unmixed and summed products, and is amplified by an op-amp (U22). The output of this amplifier is sent to the audio output, selected by a FET switch (U6), which is driven from the logic and control circuit. For a full-scale input of +10 dBm, the output will be 1.6 Volts peak-to-peak. Dynamic range is not a consideration because BFO is used for detection of CW signals.

Narrowband AM detection is provided by the DCIF, where detection is a byproduct of the bandwidth-limiting process. Detected narrowband AM arriving from the DCIF may be switched to pass through the log detector by means of a relay (K1). This will result in the same log compression characteristic that is used for wideband AM, but with a slightly different gain distribution, since the DCIF is now part of the signal path. Alternatively, another relay (K2) may switch the signal from the DCIF around both the log detector and the carrier-suppression filter, routing it directly to the envelope filter and the video output amplifier. This allows the linear gain characteristic of the DCIF to be retained, along with a dynamic range much wider than that of the wideband AM detector. In this mode the full-scale input from the DCIF, which is zero to five Volts, produces a zero to four Volt output from the video amplifier, for a net attenuation of the signal. If the log detector is switched in, then a similar overall attenuation applies, although the signal from the DCIF must be attenuated to -4 dBm full-scale before entering the log detector.

Turning to module outputs, the signal for the video output connector on the front panel of the radio is taken from the output of the video output amplifier buffer (U20) through a resistor which establishes a 50 Ohm source impedance. This driving point also provides the source for several more outputs, including the DVM module output and the AGC output, and partially for the audio output. It also drives the overload detector circuit. The output provided for the optional DVM module passes through a resistor which also provides a 50 Ohm source impedance. The output to the AGC circuits doesn't need such wide bandwidth and low noise, however, and so its source resistor is set to give it a source impedance of 750 Ohms, thus reducing the load on the video amplifier. The AGC output feeds a number of AGC amplifiers in the 21.4 MHz IF section. Likewise, the signal to the audio output is first attenuated through a resistive divider and then selected by a FET switch (U10). The other selection available for audio is the output of the BFO circuit, selected by another FET switch (U6). As mentioned above, the output from the BFO circuit is 1.6 Volts full scale, while the resistive divider on the video amplifier produces a full-scale output of 1.3 Volts. The audio output is passed to the audio amplifier circuit on the X Axis/Audio Amplifier PCB in the front panel assembly, which features a volume control and a maximum gain of about 50.

The Z axis output is driven by a separate amplifier which features on/off, gain, and inversion controls. It is also AC-coupled. Gain is set by a potentiometer on the front panel. A constant current source based on a FET (Q2) produces a voltage which is proportional to the control setting while requiring only one "hot" line and a return connection to the front panel control. This voltage drives an op-amp (U4), which develops a DC gain-setting voltage. Inversion control is provided by a FET switch (U6), set by the logic and control circuit, which acts to make the opamp inverting or non-inverting, thus producing either a positive or negative gain-setting voltage ranging from -5 to +5 Volts. The gain-setting voltage from the opamp passes through another FET switch (U6 again) which acts as an on/off switch by reducing the gain-setting voltage to zero when the switch is opened. This will attenuate the Z axis signal by about 60 dB at low frequencies, and by at least 40 dB at 8 MHz.

The gain-setting voltage forms one input for a four quadrant multiplier (U7), the other input for which is taken from the main video amplifier, from a point between the leading op-amp (U19) and the following buffer (U20), via AC-coupling capacitors (C109 and C110). The current output of the multiplier is then converted to voltage by an op-amp (U8). The voltage is then AC-coupled by a set of capacitors (C53, C55, C56), and provided with adequate current drive by a video buffer (U9). The output of the buffer is passed through a resistor to set the source impedance to 50 Ohms. The Z axis output is then routed to a connector on the rear panel of the radio.

With the Z axis amplitude control set to maximum, the amplitude at the Z axis output will be approximately 1.5 times that at the video output, not counting any DC offset at the video output. Bandwidth for each is limited by previous bandwidth, carrier removal, and video noise filtering, except that the low-end corner for the Z axis output is at about 3.8 Hz.

The overload detection circuit consists of a high-speed comparator (U5) connected to the output of the main video amplifier. A trimmer (R44) sets the threshold value, which is 4.1 Volts at the video output. The output of the comparator feeds drivers in the logic and control circuit which place the overload status on the cardcage bus.

The logic and control circuitry consists of address decoding from the cardcage bus (U13, U15), bit latches for the various controls (U14, U16), relay drivers (U12), and status return drivers (U11). There are three double-pole, double-throw relays (K1 - K3), four single-pole, single-throw relays (K4 - K7), and five single-pole, single throw FET switches (U6, U10) to control. In addition, a couple of enable bits are provided for future slideback and pulse stretch options.

The first latch controls the seven relays. It is mapped to cardcage bus address 7E(hex). Bit assignments are as follows:

Bits 0 - 3 = video filter selection:
Bit 0 = 4 MHz filter (K6, C100)
Bit 1 = 400 kHz filter (K7, C101)
Bit 2 = 40 kHz filter (K5, C99)
Bit 3 = 4 kHz filter (K4, C98)
0 = disabled
1 = enabled
Bit 4 = log amp input selection: (K1)
0 = DCIF input
1 = 21.4 MHz IF input
Bit 5 = log/lin detector selection: (K2)
0 = linear detector
1 = log detector
Bit 6 = video output selection: (K3)
0 = from 21.4 MHz detection
1 = from DCIF detection
Bit 7 = spare

In practice, when a lower frequency video filter is selected, higher filters are omitted to save power in the relay coils.

The last three relays (K1 - K3) are set to specific states for each of the various operating modes. Table 4-3 shows the various combinations.

Table 4-3: Video Relay Selection

State	Log Input Selection (K1)	Log/Lin Selection (K2)	Output Selection (K3)
Wideband Linear	DCIF (0)	Linear (0)	21.4 MHz IF (0)
Wideband Log	21.4 MHz IF (1)	Log (1)	21.4 MHz IF (0)
DCIF Linear	DCIF (0)	Linear (0)	DCIF (1)
DCIF Log	DCIF (0)	Log (1)	DCIF (1)

Relay control lines are passed through relay drivers (U12) which provide diode-clamped current sinks for the relay coils. The relays all use 5 Volt coils.

The second latch controls the FET switches and provides spare control bits for future options. It is mapped to cardcage address 7F(hex). Bit assignments are as follows:

Bit 0 = BFO enable:
0 = disable
1 = enable
Bit 1 = Z axis enable:
0 = disable
1 = enable
Bit 2 = Z axis invert:
0 = normal
1 = invert
Bit 3 = slideback enable (future option):
0 = disable
1 = enable
Bit 4 = pulse stretch enable (future option):
0 = disable
1 = enable
Bits 5 - 7 = spare

Most of the FET switches (U6) are open when the controlling latch bit is 0, closing when the bit is set to 1. Only one of the switches (U10), the one which is used to connect the BFO output to the audio output, is the other way around. This allows the same state of the same control bit to control two switches in opposite states.

Finally, the output of the detector overload circuit is routed onto the cardcage bus by a pair of tristate drivers (U11). These are connected so that their outputs are tristate (and pulled high with a resistor) when status is good (no overload), and driven active low when status is bad. Two cardcage status lines are driven: the common back end overload status line (STAT2) and a line dedicated specifically to detector overload status (STAT7). Status is sensed by the processor in the front panel assembly and also appears at the status/control connector on the rear panel of the radio.

4.5.1 Audio Output Amplifier

The audio output amplifier is part of the X axis/audio amplifier PCB (A2A4), located in the front panel assembly behind the audio and video connectors and controls. It takes its input from the audio output of the video module and drives the front panel audio output jack. In between it provides the operator with an output volume control and also mixes in the audible indicator signal from the control section (bypassing the volume control used for the signal from the video module).

The circuit consists of a preamp and a power amp. The signal from the video module passes through DC blocking capacitors (C13 and C14) and a log-taper volume control mounted on the front panel, and is routed from there to the preamp IC (U2). The combination of the DC-blocking capacitors and the volume control potentiometer produce the low-end corner frequency of the bandpass, at about 16 Hz. The preamp provides a gain of 35 for small signals and a diode limiting circuit (CR1 - CR6) which gradually reduces gain for larger signals. A capacitor in the feedback of the preamp (C10) establishes the high-end corner frequency of the bandpass at about 32 kHz. The input from the audible indicator circuit located on the interface PCB in the front panel assembly is passed through a DC-blocking capacitor (C5) and is mixed with the output of the preamp at the input of the power amp IC (U1). Gain for the input from the preamp is 1.5, while gain for the input from the audible indicator is unity. The output of the power amp is passed through a current-sensing resistor (R1) which allows the power amp to limit current to about 3 Amps. The output is routed to the front panel audio output jack, where it can drive a low-impedance (8 Ohms or less), fairly reactive load to about 4 Volts peak before the soft limiting in the preamp takes over.

The audible indicator signal is level-controlled back on the I/O PCB (A2A2). At full output it is about 2 Volts peak. Full-scale input from the video module is about 1.3 Volts peak from the linear detector and about 1.6 Volts peak-to-peak from the BFO detector. With the volume control set to maximum, gain overall gain for the signal from the video module is 52.5.

The audio amplifier shares the X Axis/Audio Amplifier PCB with the X axis output buffer, which is described in paragraph 4.8.3. The module is provided with two separate pairs of power supplies, one pair to supply the X axis buffer and the audio preamp, and one pair to supply the audio power amp. Each pair of supplies is provided with a separate return, and grounds on the module are separated from one another. The audio output jack on the front panel is isolated from the sheet metal with insulating washer, so that the audio output is completely isolated from the rest of the radio. This was done in order to prevent the high current draw at the audio output from modulating the supplies to the other modules. In addition, the audio power amp is provided with large filter capacitors (C1, C6) to reduce current surges on its supply lines. Separate regulators are provided for it (and the analog supply requirements of the control section) in the power supply.

The audio power amp IC is heatsinked to the front panel bulkhead assembly.

4.6 Synthesizer Section

The synthesizer section produces the fixed and tuneable local oscillator frequencies used for converting the signal at the receiver's input to the various intermediate frequencies. It also provides the programming frequency for the swiched capacitor filters in the DCIF. The section is implemented in the following modules:

- fixed LO synthesizer module, A1A15
- low frequency synthesizer module, A1A16
- microwave synthesizer module, A1A17
- part of the microwave RF module, A1A1
- part of the preselector module, A1A2

In addition, the synthesized frequency produced by the fixed LO module for the switched capacitor filters in the DCIF (which isn't fixed in frequency despite the name of the module) is passed to programmable dividers in the DCIF module (A1A11), which effectively act as part of the synthesizer.

The block diagram of the section is shown in figures 4-11 and 4-12.

4.6.1 Local Oscillator Usage

The receiver uses three different conversion schemes and a total of four intermediate-frequency stages (including the DCIF). The synthesizer generates the local oscillators used for these stages, as shown in table 4-4.

Table 4-4: Local Oscillator Usage

IF Frequency	LO Frequency
Band 1: 1 kHz - 250 kHz	
First IF: 3.001 MHz - 3.25 MHz	3 MHz
Second IF: 21.4 MHz	24.401 MHz - 24.65 MHz
Band 2: 250 kHz - 15 MHz	
First IF: 21.4 MHz	21.65 MHz - 36.4 MHz
Band 3: 15 MHz - 1 GHz	
First IF: 1445 MHz - 1455 MHz	1470 MHz - 2450 MHz
Second IF: 545 - 555 MHz	2 GHz
Third IF: 21.4 MHz	523.6 MHz - 533.6 MHz

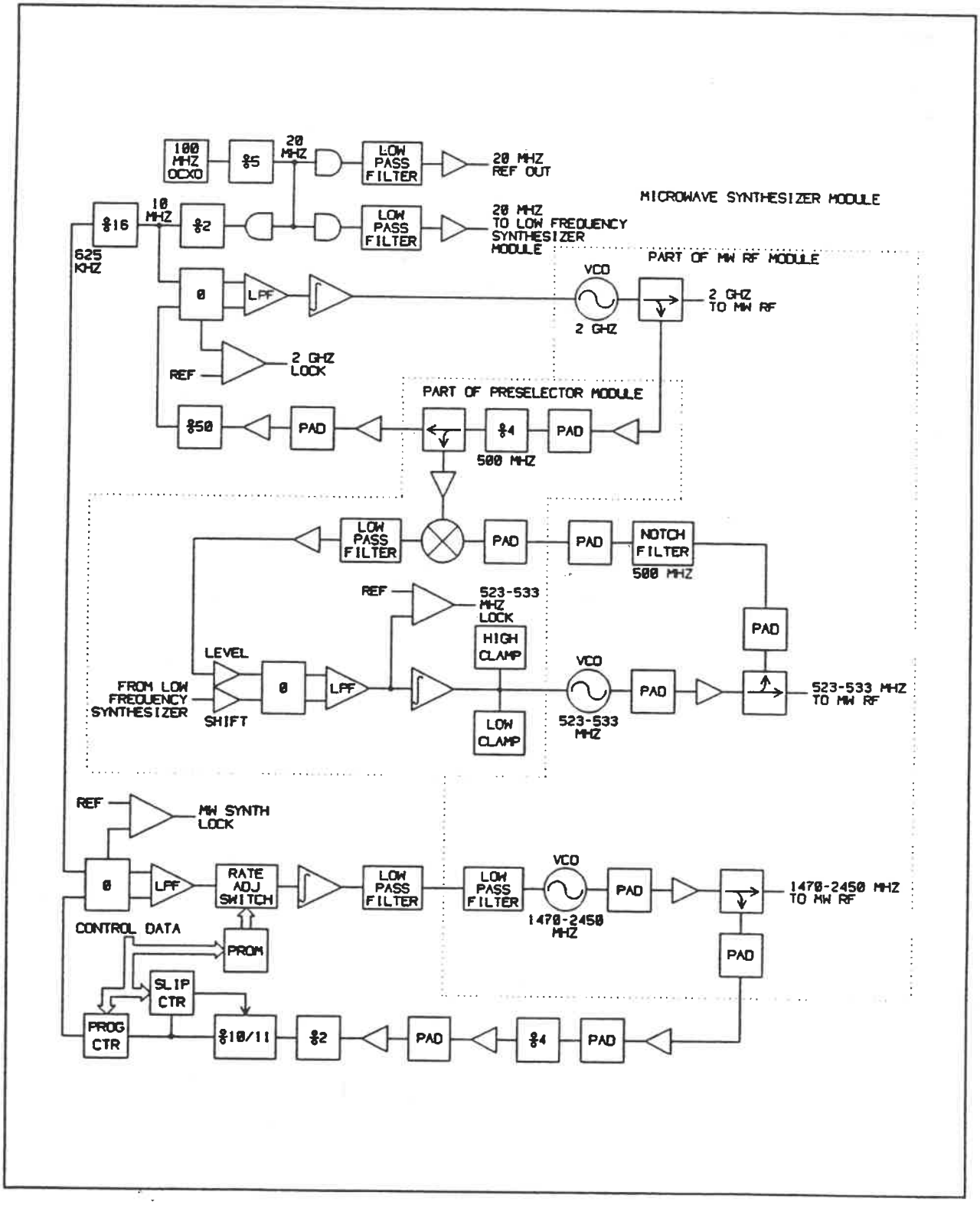

Figure 4-11: Synthesizer Section Block Diagram Part 1

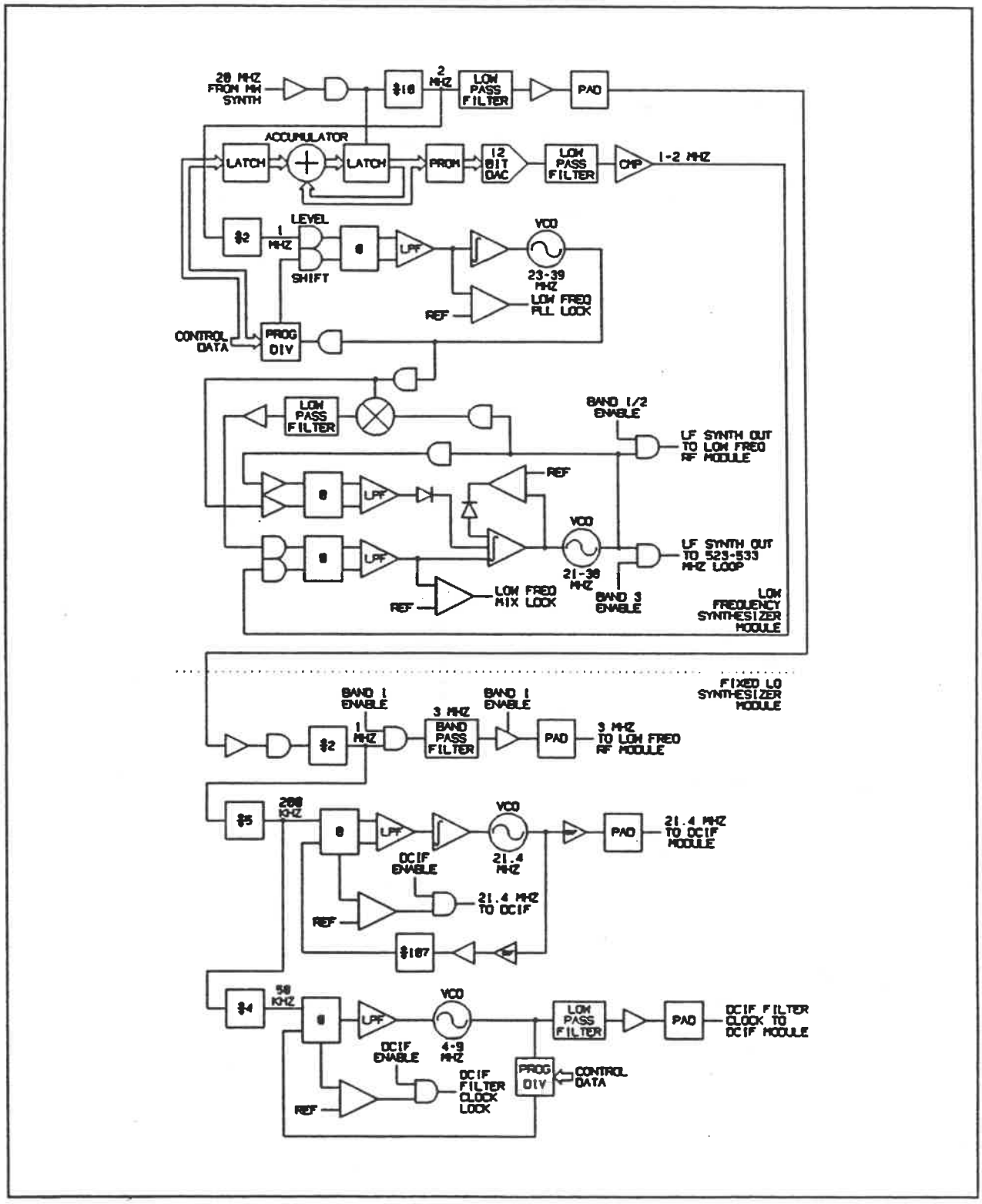

Figure 4-12: Synthesizer Section Block Diagram Part 2

In order to reduce the LO bleed-thru in the front end of the receiver when tuned between 15 MHz and 20 MHz (bottom end of band 3), the first and third LO frequencies are shifted. The first LO is moved up 5 MHz and the third LO is moved down 5 MHz so that the result is still 21.4 MHz for the third IF. This puts the L.O. bleed-thru after the upper break frequency of the first IF and before the lower break frequency of the second IF. As a result, when the receiver is tuned below 20 MHz the first LO is well out of band for the first and second IF, providing maximum LO rejection.

4.6.2 Microwave Synthesizer Module (A1A17)

This module contains the 100 MHz oven-stabilized crystal oscillator (U33) used as the reference for the entire receiver. It contains the control sections for the two microwave synthesizers, the other parts of which are located in the microwave RF module (A1A1) and the preselector module (A1A2). It generates a 20 MHz reference for the low frequency synthesizer module (A1A16), and another 20 MHz for the rear panel reference output jack. Finally, there is a cardcage backplane interface circuit.

One of the microwave synthesizers produces a fixed 2 GHz output. The other one is programmable from 1470 MHz to 2450 MHz in 5 MHz steps.

The crystal oscillator feeds an ECL digital divider (U36) which outputs 20 MHz. This is buffered by TTL (U18), amplified (U16), and padded (R48 - R50) to -10 dBm for output to the low frequency synthesizer module (A1A16). The ECL output is again buffered by TTL (U18), amplified (U17), and padded (R55 - R57) to -10 dBm for output to the rear panel reference output connector. Finally, the ECL output is buffered by TTL (U19), divided by 2 using a toggle flip-flop (U22) to yield 10 MHz, which is the reference for the 2 GHz synthesizer. The 10 MHz reference is then divided by 16 (U34) to yield 625 KHz, the reference for the programmable microwave synthesizer. A jumper selection (E5 - E7) is provided to bypass the divide-by-2, yielding a 1.25 MHz reference for future improvement of the programmable synthesizer.

The 10 MHz reference feeds the phase comparator (U24) of the 2 GHz synthesizer. The outputs of the phase comparator are filtered and combined (U21), and then integrated (U20) to form the tuning voltage for the loop VCO, which is located in the microwave RF module (A1A1A4 U4). Besides feeding the microwave module conversion circuits, the output of the VCO is padded (A1A1A4 R16 - R18, R19 - R21) to -12 dBM and sent to the preselector module, where it is re-amplified (A1A2A1 U1) and padded (A1A2A1 R2 - R4), and drives a divide-by-4 prescaler (A1A2A1 U2), yielding 500 MHz. The output of the prescaler drives a splitter (A1A2A1 U3), one output of which provides a 500 MHz fixed frequency to the 530 MHz PLL circuit. The other output is routed back to the microwave synthesizer module at -16 dBm, where it is amplified (U25, U26) and padded (R76 - R78) to drive a divider chain consisting of a divide-by-2 (U40) and two divide-by-5s (U39, U38), yielding 10 MHz at the output. This output is fed back to the other input of the phase comparator, closing the loop. Another output of the phase comparator is filtered (R72, C70) to drive a level comparator (U37) which acts as a lock detector. It drives a LED (CR9) and is fed to the status return portion of the cardcage backplane interface circuit.

The programmable microwave synthesizer is based on the 625 kHz reference. The reference drives one input of the phase comparator (U15). The outputs of the phase comparator are filtered and combined (U14), and then integrated (U13). The integrator provides the tuning voltage for the VCO (A1A1A2 U3) located in the microwave RF module. The output frequency of the VCO is nonlinear with tuning voltage, which makes the loop gain frequency-dependent. To normalize the loop gain to some extent a FET switch (U12) is used to vary the integration rate with tuned frequency. Since there are only five possible settings, this is a fairly rough adjustment. In addition, a trimmer (R30) is provided to trim out the offset of the phase comparator and combiner. The trimmer is set to minimize the reference sidebands in the output of the VCO. Since the offset contribution from the phase comparator and combiner depends on the setting of the corrective FET switch, a second FET switch (U11) is provided to scale the contribution of the trimmer as well. Both FET switches are controlled by a lookup table in PROM (U5), which is addressed by the coarse tuning data supplied to the loop dividers.

The phase comparator also drives a low-pass filter (R47, C47) and level comparator (U37) which acts as a lock detector. The output of the level comparator drives a LED (CR8) and is returned on the cardcage backpane via the interface circuit.

In the microwave RF module, the output of the VCO is padded (A1A1A2 R4 - R6) and amplified (A1A1A2 U4) to provide the 1470 - 2450 MHz LO for the microwave hardware. It is coupled by a microstrip directional coupler, padded (A1A1A2 R9 - R11) to yield -15 dBm, and returned to the microwave synthesizer module. There it is amplified (U7) and padded (R19 - R21), and ends up feeding a divide-by-4 prescaler (U9), yielding 367.5 - 612.5 MHz. The output of the prescaler is amplified (U10), padded (R15 - R17), and amplified again (U8) to drive a divide-by-2 prescaler (U4), yielding 183.75 - 306.25 MHz. There is therefore a fixed prescaling division by 8, which is what yields the 5 MHz tuning steps from the 625 kHz loop reference. The output of the second prescaler feeds the programmable divider circuit, consisting of a divide by 10/11 prescaler (U1), a decade skip counter (U3), and an 8 bit programmable divider (U6). The 10/11 prescaler divides the incoming frequency by 11 until the skip counter counts out, whereafter it divides by 10. The skip counter halts after counting out, until the programmable divider produces an output. This output reloads the skip counter and starts the cycle over again. In this way the skip counter implements the less significant part of the load data, and the programmable divider the more significant part. The output of the programmable divider drives the remaining input of the phase comparator, completing the loop.

The load data for the loop is determined by first dividing the desired output frequency by 5 MHz and forming the quotient in decimal. The last (units) digit is the load value for the skip counter. The remaining digits are then formed into a binary number. The programmable divider is loaded with one less than this number to provide the necessary ratio.

Finally there is the cardcage backplane interface circuit. This consists of a data bus buffer (U29), a pair of data latches (U27, U28), and address decoders (U30, U32). There are also tristate drivers (U31) for the status return lines, and enabling gates (U35) for them. The programmable loop lock status signal drives the backplane's common lock status line (A21) and its own individual line (B17) as well. The 2 GHz loop lock status signal drives the common lock status line as well, and also its own individual line (A16).

The two data latches store 6 bits each. One controls the programmable loop skip counter and provides an enable bit for the status return. The other controls the programmable divider, which uses 6 bits of load data. Addressing is as follows:

Address 78(hex) = skip counter latch:
Bits 0 - 3 = skip counter bits 0 - 3
Bit 4 = unused
Bit 5 = status return enable

Address 79(hex) = programmable divider latch
Bits 0 - 5 = programmable divider bits 0 - 5

Since the microwave synthesizers are only used when tuning in band 3, the status return enable bit is effectively a tuning-in-band-3 select bit. The loops remain running even when tuning is not in band 3. The PROM which controls the FET switches in the programmable loop is controlled by the five most significant bits of the programmable divider data.

4.6.3 523 - 533 MHz Mixer Loop

In tuning band 3 the signal is first converted to 1445 MHz - 1455 MHz, then to 545 - 555 MHz, then to 21.4 MHz. The conversion to the third IF requires an LO ranging from 523.6 MHz - 533.6 MHz. This is the function of the circuit described here. It consists of a mixer loop which adds the 500 MHz fixed frequency (divided from the 2 GHz fixed LO output) to the band 3 output of the low frequency synthesizer module (A1A16). The circuit is located in the preselector module (A1A2) and part of the microwave RF module (A1A1).

The output from the programmable low frequency synthesizer arrives at -10 dBm and is converted to TTL (A1 Q2) to drive one input of the phase comparator (A1 U7). This is located on a subassembly inside a can for shielding. The outputs of the phase comparator are filtered and combined (U7) and then integrated (U6) to form the VCO tuning voltage. The tuning voltage is clamped on the low side by a sensing circuit (U3, U4) which compares it to a reference set by a trimmer (R13). It is clamped on the high side by another sensing circuit (U3, U5) set by another trimmer (R14). The tuning voltage drives the VCO (A1A1A6 U3) located in the microwave RF module. The output of the VCO is padded (A1A1A6 R8 - R10) and amplified (A1A1A6 U2) to drive a splitter (A1A1A6 U1). One output of the splitter drives the signal conversion mixer, while the other one is padded (A1A1A6 R4 - R6), high-pass filtered (A1A1A6 L1, T1, T2, C1, C3) to provide reverse isolation from the 500 MHz fixed frequency, and padded again (A1A1A6 R1 - R3) to -12 dBm, at which level it is returned to the preselector module. There it is padded once more (A1 R9 - R11) and mixed (A1 U5) with a 500 MHz fixed frequency picked off from the 2 GHz fixed LO. The 2 GHz fixed LO contains a divide-by-4 preselector (A1 U2) followed by a splitter (A1 U3). One output of the splitter is padded (A1 R5 - R7) and amplified (A1 U4) to provide the 500 MHz input to the mixer. The output of the mixer is filtered (A1 L4, L5, C13, C15, C37) to select the difference component, and then amplified (A1 U6) and converted to TTL (A1 Q1) to drive the other input of the phase comparator, completing the loop.

The output needs to be 523.6 - 533.6 MHz to properly convert the incoming 545 - 555 MHz signal to 21.4 MHz. The fixed input to the mixer contributes 500 MHz, so the programmable low frequency synthesizer needs to be tuned in the range of 23.6 MHz - 33.6 MHz in band 3.

4.6.4 Low Frequency Synthesizer Module (A1A16)

This module contains a direct digital synthesizer (DDS), settable from 1 to 2 MHz, a tuneable phase locked loop programmable from 19 - 38 MHz, a mixer loop which combines the output of the programmable loop with the output of the DDS, a 2 MHz pickoff to provide a reference for the fixed LO synthesizer module (A1A15), and a logic interface for the cardcage backplane. The mixer loop is provided with safety features to ensure that it is always in the proper relationship to its two inputs.

The reference for the module comes in at -10 dBm from the microwave synthesizer (A1A17) module. It is amplified (U2) and then squared up by a logic gate (U3). This provides the clock for the DDS. It is also divided by 10 using a digital bi-quinary divider (U4), producing 2 MHz. This is filtered (C4, L31, C115), amplified (U1), and then set to -10 dBm using a pi network (R2 - R4). This is sent to the fixed LO module, where it is used as the reference for the 3 MHz multiplier, the 21.4 MHz fixed LO used by the DCIF, and the DCIF filter clock. The 2 MHz output from the divider is also divided again by 2, using the other section of the bi-quinary divider (U4), yielding 1 MHz. This is the reference for the programmable loop.

The direct digital synthesizer is contained mostly in an LSI circuit (U5). This IC contains two duplicate implementations, of which only one is used by the module. The circuit consists of a 32 bit accumulator, plus latches. There are four input latches, each connected to the incoming data bus. Data is loaded one latch at a time, determined by the applied address. When all four are loaded the set can be applied simultaneously to a second latch, 32 bits wide, by a strobe. This 32 bit latch forms one input of the accumulator. The accumulator consists of a 32 bit adder and output latch, with the output of the latch wrapped around to become the other input. the strobe for the output latch is supplied by the applied reference clock, which the module supplies at 20 MHz as described above. If the value loaded into the input latch is determined to be the fraction of the output frequency expected with each reference clock, the circuit then becomes a phase accumulator and the output latch is an indication, in encoded digital form, of the current phase of the output waveform.

The LSI circuit contains the phase accumulator and a lookup table. The output latches of the phase accumulator supply a 12 bit wide lookup table in ROM which provides the encoded values for a sine wave (actually in cosine form so that the waveform will be at its endpoints when the accumulator rolls over, rather than at the more sensitive zero crossings). The remainder of the DDS consists of a 12 bit latch (U6, U7), strobed by the LSI circuit, which acts to deskew the data. The latches are followed by a high-speed 12 bit DAC (U9), the output of which is a stairstep approximation of a sine wave. The stairstep is at the reference frequency of 20 MHz, while the sine wave is at a frequency determined by both the reference frequency and the value loaded into the input latches. The DAC is followed by a low-pass filter (A3 L1 - A3 L3, A3 C1 - A3 C3) to remove the stairstep, and a comparator (A3 U1) to square up the result. The filter and the comparator are located on a subassembly (A1A16A3) inside a can for shielding. The output of the comparator forms one of the inputs for the mixer loop.

The DDS is set to range from 1 - 2 MHz. The output is the value loaded into the input latches, divided by 2^32, times 20 MHz, or

$$Freq = \frac{N}{214.7483648}$$

in Hz, where N is the load value. Resolution is sufficient to set the frequency to within a small fraction of 1 Hz.

The 1 MHz reference for the programmable phase locked loop is derived from the 20 MHz reference from the microwave synthesizer module, as described above. The reference is converted to ECL logic levels (U16) and feeds one input of the phase comparator (U17). The other input of the phase comparator comes from an 8 bit programmable divider (U12), again converted to ECL levels (U16 again). The outputs of the phase comparator are filtered and combined (U30), and then integrated (U31). The filtered and combined signal also drives a window comparator (U27) which acts as a lock detector. The output of the window comparator drives an LED (CR1) and the bus interface logic described below. The integrated output forms the tuning voltage for the VCO, which is located on a subassembly (A1A16A1) inside a can, for shielding. This subassembly has four outputs, three of which are used, and two enable inputs, neither of which is used. One output is squared up by a comparator (U14) and drives the programmable divider (U14). The other two feed the mixer loop.

A trimmer (R36) is provided to trim out the offset of the phase comparator, combiner and integrator. The trimmer is set so that the reference sidebands in the VCO output are minimized.

The frequency of the programmable loop is set according to the equation

$$Freq = (N+1) * 1 \text{ MHz}$$

in 1 MHz steps, where N is the divider load code. The legal range is 19 to 38 MHz.

The mixer loop has as its inputs the DDS output and the programmable PLL output. The output of the mixer loop is the difference between them, so that it can range from 17 to 37 MHz with resolution to a small fraction of 1 Hz.

The reference for the mixer loop phase comparator (U19) is fed by the DDS output, converted to ECL logic levels (U18). The outputs of the phase comparator are filtered and combined (U20) and then integrated (U21). The filtered and combined signal feeds a window comparator (U27) which acts as a lock detector. The output of the window comparator drives a LED (CR2) and the bus interface logic described below. The integrated output forms the tuning voltage for the loop VCO, located on a subassembly (A1A16A2) located inside a can, for shielding. This subassembly is identical to the one used for the programmable loop, but in this case all four of the outputs and both of the enables are used. One output is sqared up by an amplifier (U29) running in saturation. The output of this amplifier drives a transformer (T1) with a 13:1 impedance ratio. The transformer provides a 50 Ohm drive for the LO input of a mixer (U32) at about +6 dBm. The other input of the mixer is driven by the output of the programmable PLL through a pad (R81 - R83) which is set to minimize the unwanted mixing products at the output. The output of the mixer is low-pass filtered (L27, L28, C95 - C97) to extract the difference product. The filter feeds another amplifier (U33), also running in saturation, which in turn drives another 13:1 transformer (T2), which drives the other input of the phase comparator through a length of 50 Ohm line (W2) and an ECL level converter (U18 again).

A trimmer (R58) is provided to trim out the offset of the phase comparator, combiner and integrator. The trimmer is set so that the reference sidebands in the VCO output are minimized.

The low-pass filter following the mixer is cut to about 2.5 MHz. Two aspects of the mixer loop are therefore worth noting:

- If the mixer VCO is more than 2.5 MHz away from the programmable loop VCO then the mixer loop is open, since the mixer output will be cut off by the filter which follows it. This may be the case at powerup.

- The mixer loop may lock on either the sum or the difference of the programmable loop and the DDS.

Additional circuitry has been provided to ensure that the mixer loop locks and operates in the correct orientation. A phase comparator (U25) compares the buffered (U26) output of the mixer loop to the buffered (U28) output of the programmable loop. The outputs of the phase comparator are filtered and combined (U24). The filtered and combined output drives the mixer loop integrator so that if the mixer loop frequency is ever higher than that of the programmable loop, the sensing circuit will then force the mixer loop VCO frequency down.

A comparator (U23) compares the mixer loop VCO tuning voltage to a trimmable reference (R68). It senses when the VCO is tuned below its legal minimum. When it triggers it charges a capacitor (C85) which then feeds the loop integrator, forcing it to tune the VCO higher as it slowly discharges.

If the mixer loop VCO is tuned more than 2.5 MHz below the programmable loop, but still within its legal range, the mixer filter will block the difference frequency, opening the loop. However, the loop phase comparator will then see no input from the filter, which it interprets as zero frequency, a too-low condition. It will therefore increase the VCO frequency in normal fashion, until the loop locks as usual.

There are two more outputs from the mixer loop VCO subassembly, each with its own enable input. One is used for the band 3 tuning and is delivered to the preselector module (A1A2) through a pad (R99 - R101) which sets the level to -10 dBm. The other is used for band 1 and 2 tuning and is delivered to the low frequency RF module (A1A5), again at -10 dBm. The enable lines are driven by the cardcage backplane interface circuitry described below.

Overall, the output frequency of the module is

$$\begin{aligned} Freq_{OUT} &= Freq_{PLL} - Freq_{DDS} \\ &= [(N_1 + 1) * 1\ \text{MHz}] - \left[\left(\frac{N_2}{214.7483648}\right) * 1\ \text{Hz}\right] \end{aligned}$$

where N_1 is the PLL load code and N_2 is the DDS load code.

The cardcage interface circuitry consists of a data bus buffer (U11), a data latch (U10), address decoding (U8, U13, U15), and tristate drivers (U22) for the status return lines. Lock detection from the programmable loop drives the backplane's common lock status line (A21) and its own discrete status line (A15). Lock detection from the mixer loop also drives the common lock status line (A21), and again its own discrete status line (B15).

The DDS IC requires 32 consecutive addresses. These are allocated to bus addresses 00(hex) - 1F(hex). The data latch is redundantly mapped into addresses 0E(hex)/1E(hex) within the address space of the DDS. This is the address which strobes the second stage input latch of the DDS, allowing the accumulator input data, which must be loaded in four pieces, to be applied to the accumulator simultaneously. By placing the data latch at this address as well, the programmable loop, the load value for which is supplied by the data latch, may also be updated at the same time, since data applied to the DDS strobe address is unimportant.

Data latch bit assignments are as follows:

Bits 0 - 5: programmable loop divider code
Bits 6 - 7: band select code:
- 00 = band 1 enable
- 01 = band 2 enable
- 10 = band 3 enable
- 11 = unused

The band select code is decoded with a spare section of one of an address decoder IC (U15). The band 1 and band 2 selects are ORed (U3) to provide a combined band 1/2 select line. The band 1/2 select drives the band 1/2 output enable of the mixer loop VCO subassembly. The band 3 select does the same for the VCO band 3 output enable.

4.6.5 Fixed LO Synthesizer Module (A1A15)

The low frequency RF input module (A1A5) requires a 3 MHz fixed LO to upconvert the low frequency input by that amount. This is provided by the fixed LO module at -3 dBm. The 20 MHz reference from the low frequency synthesizer/DDS module (A1A16) arrives at -10 dBm and is amplified (U2) and then squared up by a logic gate (U3). It is then divided by 2 using a toggle flip-flop (U19), yielding 1 MHz. The output is passed through an enabling gate (U3 again) and filtered (L7 - L11, C20 - C25) for the third harmonic at 3 MHz. Proper operation of the filter depends on the input level, set by a resistive divider (R24, R25). The result is amplified (U8) and set to -3 dBm by a pi network (R26 - R28). This provides the output for the low frequency RF module. Everything past the enabling gate is located inside a can, for shielding.

The DCIF uses a fixed 21.4 MHz reference to convert the 21.4 MHz IF directly to baseband. The clock circuit, located in the Fixed LO module (A1A15), is a single phase-locked-loop. The reference for the loop is taken from the 3 MHz multiplier circuit described above at the point at which it is at 1 MHz. From there it is divided by 5 to form 200 kHz, using a bi-quinary digital divider (U6). This is the reference for the loop. The phase comparator (U18) compares the reference to the output of an 8 bit divider (U4). The output of the phase comparator is filtered (U16) and integrated (U15) to form the control voltage for a VCO based on a transistor (A1 Q1) and a tuning diode (A1 CR2). The output of the oscillator is buffered (A1 U2) off of the module at -10 dBm and is sent to the DCIF module (A1A11). It is also buffered (A1 U1) and amplified (A1 U3) to feed the divider (A1 U4) which feeds the phase comparator. The divider provides a ratio of 107, which establishes a VCO output of 21.4 MHz in phase lock. A low-pass filter (R43, C53) and comparator (U17) connected to the phase detector provides lock detection. The output of the comparator drives a LED (CR2) and backplane status lines (the common lock line at A21 and the 21.4 MHz-specific line at A14) through an enabling gate (U13) and tri-state drivers (U14). The VCO, its output buffers and amplifier, and the loop divider comprise a subassembly (A1A15A1) located between vertical shielding walls, for isolation.

The DCIF also requires a programmable timebase for its switched-capacitor filters. This is provided in the form of a phase locked loop on the fixed LO module and programmable dividers on the DCIF module. The phase locked loop can range from 4.8 MHz to 8.8 MHz. The reference for the loop is taken from the 200 kHz reference used by the fixed 21.4 MHz phase locked loop and is divided by 4 using the remaining sections of the bi-quinary counter (U6), yielding a 50 kHz reference for the loop. The phase comparator (part of U5) compares this to the output of an 8 bit digital counter (U4). The output of the phase comparator is filtered and integrated (part of U5 again) and supplies the control voltage for the VCO (still another part of U5). The output of the VCO feeds the divider, and is also filtered (C4, L17, C54), amplified (U1), and set to -10 dBm by a pi network (R1 - R3) to feed the DCIF. The divider may be set from about 96 to 176 to provide the required range of outputs, in 50 kHz steps. A low-pass filter (R15, C13) and comparator (U7) connected to the output of the phase comparator provides lock detection. The output of the comparator drives a LED (CR1) and backplane status lines (the common lock line at A21 and the DCIF filter clock-specific line at B14) through an enabling gate (U13) and tri-state drivers (U14).

The backplane interface for the module consists of a data bus buffer (U10) and address decoding (U9, U12), plus a two bit control latch (U11). One bit is set according to whether tuning is in band 1. When set, the bit is used to enable the 3 MHz multiplier through its enabling gate (U13). It also is used to switch the supply to the 3 MHz output amplifier (U8) on and off via a transistor switching circuit (Q1 - Q3). The other control bit is set according to whether the DCIF is in use. When set it is used to enable the DCIF filter clock VCO (U5) and divider (U4), the fixed 21.4 MHz divider (A1 U4), and the enabling gates (U13) for the status line drivers. It is also used to switch the supply to the 21.4 MHz VCO (A1 Q1) on and off via a transistor switching circuit (Q4 - Q6).

The data bus feeds the control latch and the DCIF filter clock loop divider (U4). The address usage is as follows:

Address 70(hex) = control latch:
- bit 0 = band 1 select
- bit 1 = DCIF select
- bits 2 - 7 = unused

Address 70(hex) = DCIF filter clock divider ratio
- bits 0 - 7 = ratio bits 0 - 7

The output of the DCIF filter clock will be

$$Freq = (255 - N) * 50\ \text{kHz}$$

where N is the code sent to the divider address.

4.7 Cardcage Backplane (A1A20)

The cardcage backplane is a passive implementation which provides power and digital control signals for the plug-in modules and the microwave RF module (A1A1). The backplane provides 16 sockets for plug-in modules, numbered J2 - J17. The assembly numbers of the plug-in modules match the socket that they plug into (e.g., the video module, A1A9, plugs into the J9 socket of the backplane). J1 is the power and control header for the microwave RF module, which, while it doesn't plug directly into the backplane, fits adjacent to it and is connected to it via a discrete-wire pigtail. See table 4-5.

Table 4-5: Cardcage Backplane Connector Usage

Connector	Usage
J1	Microwave RF Module (A1A1) Cable
J2	Preselector Module (A1A2)
J3	Spare
J4	Spare
J5	Low Frequency RF Module (A1A5)
J6	21.4 MHz IF Amplifier Module (A1A6)
J7	Spare
J8	21.4 MHz IF Filter Module (A1A8)
J9	Video Module (A1A9)
J10	Spare
J11	DCIF Module (A1A11)
J12	Spare
J13	Spare
J14	Spare
J15	Fixed LO Synthesizer Module (A1A15)
J16	Low Frequency Synthesizer Module (A1A16)
J17	Microwave Synthesizer Module (A1A17)
J18	Control Section Interface Cable

Power is provided from the power supply via discrete wires, passing through the cardcage sidewall via filtered feed-thrus. Some supplies are shared with the front panel assembly. Power supply voltages available on the backplane include:

- +5 VDC and separate return
- +/- 8 VDC and separate return
- +/- 15 VDC and separate return
- +50 VDC and separate return

Note that while the return lines for the various power supply voltages are kept separate by the backplane, the microwave module requires +5 VDC, -8 VDC, and +15 VDC, but uses only the +5 return and the +/- 15 VDC return. Furthermore, these two returns are bridged together inside the module.

The sockets for the plug-in modules consist of 64 contact, double-row DIN connectors. Power distribution and connections to the front panel assembly account for most of the contacts, which for these signals are bussed in common across the backplane. The remaining lines are available for use by discrete logic signals between specific sockets, and it is this set of connections which prevents any plug-in module from working in any socket.

The interface to the front panel assembly is in the form of a 37 conductor ribbon cable, attaching to the backplane at J18. All of these lines are bussed across the backplane as a single group, and are located on inside layers of the backplane, shielded on top and bottom by the +5 VDC and return planes. The driven lines are active only when a command is being issued to a plug-in module, and the status return lines are active only when a status change occurs, so most of the time all of the lines are in static states, which reduces noise.

The standard connector pinout for the plug-in modules is shown in table 4-6. The current selection of dedicated traces is shown in table 4-7. The usage of the status signal lines is shown in table 4-8.

Table 4-6: Backplane Connector Standard Pinout

Contact	Usage	Contact	Usage
A1	-15 VDC	B1	-15 VDC
A2	15 RTN	B2	15 RTN
A3	+15 VDC	B3	+15 VDC
A4	-8 VDC	B4	-8 VDC
A5	8 RTN	B5	8 RTN
A6	+8 VDC	B6	+8 VDC
A7	+50 RTN	B7	+50 VDC
A8	(Available)	B8	(Available)
A9	(Available)	B9	(Available)
A10	(Available)	B10	(Available)
A11	(Available)	B11	(Available)
A12	Status 18	B12	(Available)
A13	Status 16	B13	Status 17
A14	Status 14	B14	Status 15
A15	Status 12	B15	Status 13
A16	Status 10	B16	Status 11
A17	Status 8	B17	Status 9
A18	Status 6	B18	Status 7

Table 4-6: Backplane Connector Standard Pinout (Continued)

Contact	Usage	Contact	Usage
A19	Status 4	B19	Status 5
A20	Status 2	B20	Status 3
A21	Status 0	B21	Status 1
A22	Clear*	B22	Thresh
A23	Address 6	B23	Write*
A24	Address 4	B24	Address 5
A25	Address 2	B25	Address 3
A26	Address 0	B26	Address 1
A27	Data 6	B27	Data 7
A28	Data 4	B28	Data 5
A29	Data 2	B29	Data 3
A30	Data 0	B30	Data 1
A31	+5 RTN	B31	+5 RTN
A32	+5 VDC	B32	+5 VDC

Note: "Available" denotes a contact which has no standard, bus-wide usage. It may be dedicated for use between specific connectors. "Thresh" is reserved for the threshold indicator output of the AM slideback function.

Table 4-7: Backplane Connector-Specific Pinout

Contact	Starting Connector	Ending Connector	Usage
A8	J2	J6	Wideband Enable*
B8	--	--	(Unused)
A9	J2	J6	Band 3 Enable*
B9	J6	J8	80 kHz BW Enable*
A10	J6	J8	300 kHz BW Enable*
B10	J6	J8	1 MHz BW Enable*
A11	J6	J8	4 MHz BW Enable*
B11	J6	J8	15 MHz BW Enable*
B12	J5	J6	Band 1/2 Enable

Note: In the above table entries, a trace is placed on the backplane which connects the indicated contact on the "starting" connector, the "ending" connector, and all connectors in between. The "wideband enable*" and "band 3 enable*" traces are also delivered to J1, the microwave module power and control header.

Table 4-8: Backplane Status Line Usage

Contact	Signal	Usage
A21	Status 0	Combined Synthesizer Lock
B21	Status 1	Combined Front End Overload
A20	Status 2	Combined Back End Overload
B20	Status 3	Front End Underload
A19	Status 4	(Spare)
B19	Status 5	Video Overload
A18	Status 6	DCIF Overload
B18	Status 7	21.4 MHz IF Overload
A17	Status 8	RF Overload
B17	Status 9	Prog MW Synthesizer Lock
A16	Status 10	2 GHz Synthesizer Lock
B16	Status 11	530 MHz Mixer Loop Lock
A15	Status 12	LF Prog Synthesizer Lock
B15	Status 13	LF Mixer Loop Lock
A14	Status 14	21.4 MHz Synthesizer Lock
B14	Status 15	DCIF Filter Clock Lock
A13	Status 16	(Spare)
B13	Status 17	(Spare)
A12	Status 18	(Spare)

4.8 Control Section

The control section administers the operation of the receiver. Taking its inputs from the front panel and the IEEE-488 interface, it supplies control signals to the receiver's relays, switches, amplifiers, attenuators, and synthesizers, and status information to the front panel displays, the rear panel status outputs, and again to the IEEE-488 interface. Physically, the control circuitry resides on the processor PCB, the interface PCB, and the switch/display PCB, all located in the front panel assembly. Modules in the cardcage, such as the DCIF and video modules, contain latches and buffers to interface data to and from the control section as well. Figure 4-13 is a block diagram of the control section.

The receiver has three main control modes:

- manual mode, in which all functions are controlled by the front panel.
- remote mode, in which tuned frequency, IF bandwidth, input attenuation, gain, log/linear detector selection, and other functions are controlled by the IEEE-488 interface.
- MDC mode, provided for operation in conjunction with the companion R-1180 microwave down-converter, in which the downconverter's RF input selection, RF input attenuation, and frequency tuning are controlled by the R-110 over the IEEE-488 interface.

In remote mode the remote indicator on the front panel is illuminated. In MDC mode the MDC mode indicator on the front panel is illuminated. The two modes are mutually exclusive, so much so that if one is selected the operator must then manually disable it and enable the other one before the other one will operate.

A block diagram of the control section is shown in figure 4-13.

4.8.1 Switch/Display PCB (A2A1)

The switch/display PCB (A2A1) is attached directly to the back of the receiver's front panel, using standoffs. All of the radio's pushbuttons, displays, and indicators are directly connected to this PCB. The frequency tuning and IF gain controls are connected to it as well, via pigtails.

The tuning and gain controls are quadrature optical shaft encoders attached to the front panel and connected to the switch/display PCB with 4-conductor ribbon cables (J1, J2). Each control requires four connections in order to operate. Two of these are +5 Volts and ground. The other two are the encoder outputs, and the relationship in which pulses occur on them determines the direction of rotation of the shaft. The encoder produces about 200 pulses on each line per rotation of the shaft. These occur 90 degrees out of phase from one another, so that if one is used as a trigger then the other may be used as a directional indicator, since it will be high for rotation in one direction and low for rotation in the other. The two signal lines from each encoder are delivered to the interface PCB (A2A2) for processing.

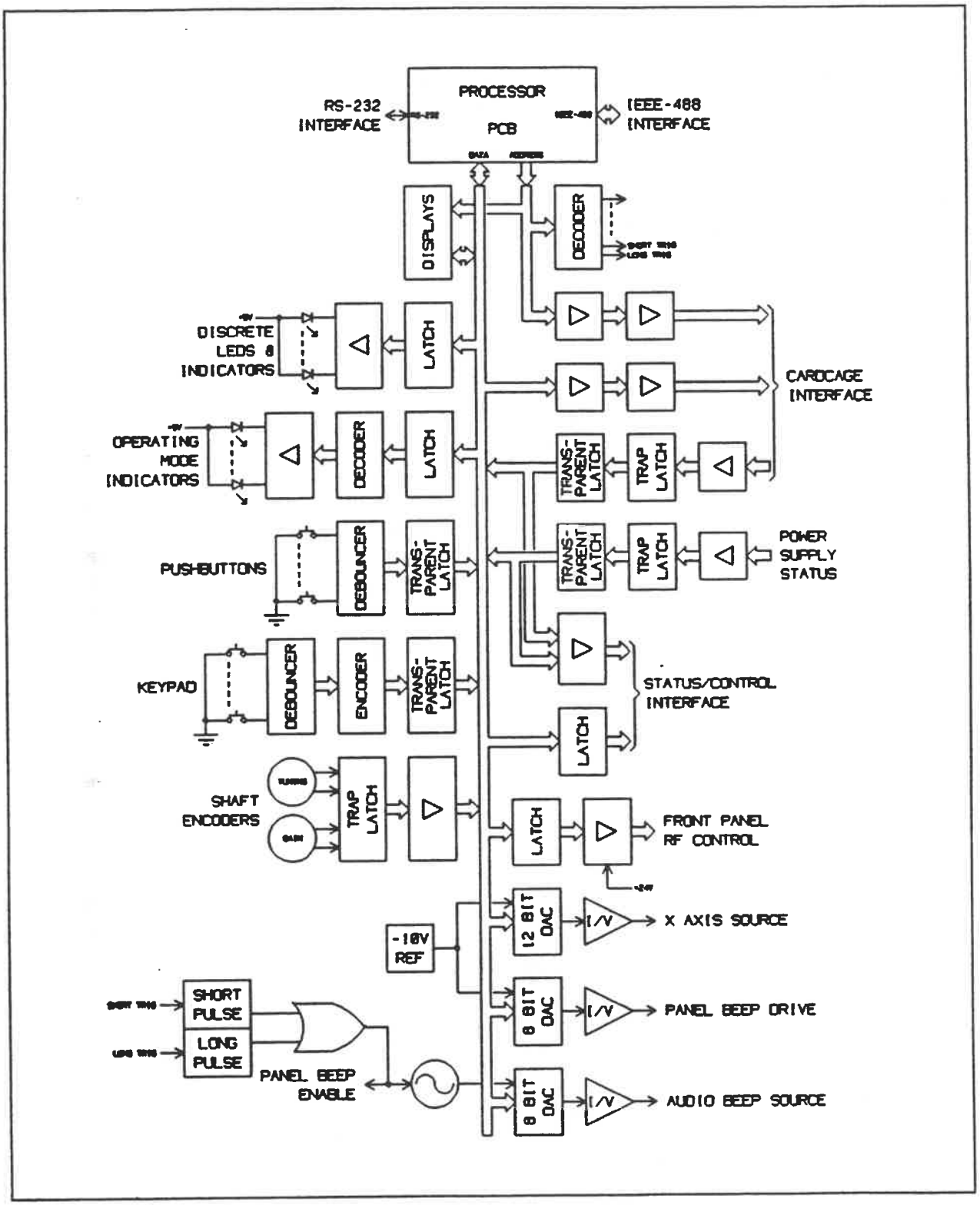

Figure 4-13: Control Section Block Diagram

Indicators consist of single LEDs mounted within some of the pushbuttons (S1, S2, S7 - S9, S14 - S16, S32, S34), and rectangular LED lightbars above and below the general-purpose alphanumeric displays (DS7 - DS34). Displays are scanned LED matrices, packaged four per module (DS1 - DS6). All are mounted directly on the PCB, along with the pushbuttons (S1 - S11, S14 - S32, S34). Each LED indicator and lightbar is driven separately by the interface PCB, through high-current bus driver ICs (U1, U2, U4 - U6). Note however that the operating mode lightbars (the row below the tuning display) are mutually exclusive in use and are therefore driven through a decade decoder (U3), so that only one of them may be illuminated at any given time. A four bit code is delivered from the interface PCB to control the decoder, and the coding is shown in table 4-9. The display modules are "intelligent" and are driven using data, address, and control buses from the interface PCB. The pushbuttons are single-pole, single-throw components with one side connected to ground. A signal line from the other side of each is delivered to the interface PCB. The front panel audible indicator (SP1), a piezo transducer, is also provided. It too is controlled from the interface PCB, through a switching transistor (Q1).

Table 4-9: Operating Mode Indicator Codes

Code	Indicator
0	"TUNE"
1	"START"
2	"STOP"
3	"STEP"
4	"RATE"
5	"SCAN"
6	"STORE"
7	"RECALL"
8	"GPIB"
9	"REMOTE"

Each of the alpha displays provides four characters. The characters are made up of rectangular 5 x 7 matrices of LEDs, which are scanned automatically in two dimensions by the IC to produce the desired ASCII character. This scanning, combined with the fact that 840 individual LEDs are being driven, results in a significant and highly modulated current draw. Filtering in the form of capacitors (C1, C8, C17 et al) and an inductor (L1) are provided in order to keep as much of this as possible off of the supply and ground lines. In addition, the alpha displays use separate +5 Volt and ground planes, isolated from those used by the rest of the PCB and supplied by separate wiring from the power supply. Finally, conductive filter screens are embedded in the display windows on the front panel to limit radiation from the radio. The brightness of the displays is settable to 0%, 25%, 50%, or 100%, so if necessary the amount of display noise may be reduced in special testing situations by turning off the displays for the duration of the test. Since brightness is set by varying the duty cycle of the scanning within the displays, only the full-off setting will effectively reduce the noise. The scanning frequency is generated internally by one of the displays (DS1) and is sent from there to the other five.

The switch/display PCB mates with the interface PCB using 50 and 60 pin headers (P1, P2).

4.8.2 Interface PCB (A2A2)

The function of the interface PCB (A2A2) is to connect the intelligence of the processor PCB (A2A3) to the front panel controls and indicators, the cardcage hardware, and the rear panel status/control connector. The two main external interfaces, the IEEE-488 and the RS-232, reside directly on the processor PCB. One additional function of the interface PCB is to provide the source signal for the X axis output. The interface with the processor PCB consists of power and a control bus. The bus has eight bidirectional data lines, eight unidirectional address lines, and separate read, write, and clear lines. An interrupt request line is also provided in the interface, but is currently unused.

All of the front panel's pushbuttons, indicators, and displays are mounted on the switch/display PCB (A2A1), and the frequency tuning and IF gain control shaft encoders are connected to it. Signals from the pushbuttons and shaft encoders are returned as discrete lines. Signals destined for the LEDs mounted inside the pushbuttons and lightbars are also delivered as discrete signals, except that those destined for the mode indication lightbars (located below the tuning display on the front panel) are delivered as a four bit code, to be decoded on the switch/display PCB. The tuning, attenuation, gain, and bandwidth displays are made up of intelligent ICs, which have data, address, and control lines delivered to them by the interface PCB.

The front panel's pushbutton switches are single-pole, single-throw parts with one side connected to ground. Inputs from these switches must be debounced, which is provided for by ICs (U20, U27, U29, U35, U37, U39) which act as shift registers. Data from a switch is shifted and all stages inside are compared to one another. When all are in the same state it is judged that the switch has attained a stable state and that state is presented at the output. The debouncers generate their own shift clock, set by an external capacitor (C23, C39, C42, C49, C52, C55). Data from the debouncers which service the keypad pushbuttons ("0" - "9", "H", "K", "M", "C", ".") are encoded by a pair of octal priority encoders (U33, U41), whose outputs are gated together (U31) to form a single four-bit code. The priority and code for each pushbutton is shown in table 4-10. When a particular keypad pushbutton is pressed, all those of lower priority are locked out, while each of those of higher priority is able to supercede the one being pressed if it too is pressed. If no button is pressed then the lowest priority input takes over. The code produced is the complement of the priority of the highest priority button being pushed. This scheme was chosen for its static nature (no scanning clock required) and low parts count rather than for any advantage to the prioritization of the pushbuttons.

Table 4-10: Keypad Key Codes

Key	Priority	Code
None	0 (low)	15
"0"	1	14
"1"	2	13
"2"	3	12
"3"	4	11
"4"	5	10
"5"	6	9
"6"	7	8
"7"	8	7
"8"	9	6
"9"	10	5
"."	11	4
"H"	12	3
"K"	13	2
"M"	14	1
"C"	15 (high)	0

The code from the keypad encoder, plus the debounced signals from the other pushbuttons which aren't encoded, are routed to the interface PCB's internal data bus via tristate buffers (U19, U26, U38).

Each of the two shaft encoders on the front panel, when rotated, produces two pulse trains in quadrature, the phase relationship between the two depending upon the direction of rotation. This can be interpreted as a trigger line and a direction line. Two flip-flops (U15, U16) are used for each encoder to sense rotation and direction. Both flip-flops are clocked by the trigger line. One is always set high to indicate that a trigger has occurred, while the other latches the state of the direction line at the time the trigger occurs. All four of the resulting latch lines are routed to the data bus through tristate drivers (U17). When the data is read over the bus the driver is enabled with a strobe line. The end of the strobe pulse is used to generate a clear pulse for the four latches. The reset pulse is generated by setting a flip-flop (U18) and then using its output to immediately reset it, delayed through a gate (U31). This readys the latches for the next trigger from the shaft encoders.

Latches on the data bus (U18, U21, U22, U30, U32) store data which controls the front panel discrete LEDs and lightbars. One set of lightbars, those used to indicate the current operating mode of the radio (the row located below the tuning display on the front panel) are mutually exclusive, so that only one may be illuminated at a time. A decoder is provided on the switch/display PCB to ensure this, so our latch here supplies the decoder with a four bit code. Control signals for the LEDs and lightbars pass through current drivers on the switch/display PCB, so no heavy loading is present here.

The tuning, attenuation, gain, and bandwidth displays consist of intelligent modules which provide four characters each. These modules require a bus interface similar to that used internally by the interface PCB. Each IC requires eight data lines, three address lines, a chip select line, a clear line, and read and write strobes. The chip selects are derived as part of the address decoding on the interface PCB, while the rest are connected directly to the interface PCB's internal bus. A character is displayed by sending its ASCII code to the appropriate address. If the eighth data bit is set as well then the "attribute" (such as blinking) for that character is enabled as well. Brightness is settable through one of the addresses as well.

The cardcage backplane bus is an extension of the interface PCB bus. However, the backplane bus data lines are unidirectional (write only) and only seven address lines are provided. Tristate buffers (U6, U28) are placed between the interface PCB bus and the lines leading to the cardcage. These buffers are enabled only when the eighth address bit is low. This effectively dedicates half of the available interface addresses, 00(hex) to 7F(hex), to the cardcage. These lines do not go directly to the cardcage, but pass first through further buffering on the processor PCB.

The backplane bus also provides eighteen discrete status return lines. The standard protocol on these lines is that a high line indicates good status, while a low line indicates bad status. Bad status may be very short-lived, but must still be detected, and so a set of status capture latches (U7 - U14, U46) are provided. There are eighteen independent flip-flops, each of which may be preset by a particular status line going low. Outputs from the flip-flops are routed to the interface PCB's internal bus through tristate buffers (U34, U36, U47). The flip-flops attached to a given buffer are written low at the end of the read strobe for that particular buffer. If the status is still bad, then the preset overrides the write to the flip-flop and it remains set. In addition, the first four status lines are also passed to the rear panel status/control connector through another buffer (U40) without being latched. The more important cardcage status signals have been assigned to these lines (unlock, front end overload, back end overload, and front end underload).

Four discrete status signals are also received from the power supply, although only three are currently used (AC high, AC low, and DC regulation). These are treated like the cardcage status lines, presetting flip-flops (U44, U45) when low, and the outputs of the flip-flops being routed to the data bus through a tristate buffer (U47). These four lines are also passed, unlatched, through a buffer (U40 again) to the rear panel status/control connector.

The ICs which buffer data onto the data bus are actually tranparent latches. While they normally track their inputs, during read strobes they freeze their outputs in order to ensure a stable reading.

Sixteen more lines are passed to the rear panel status/control connector, but these are set by latches (U42, U43) connected to the interface PCB bus. They allow the microprocessor to indicate its internal status, or allow it to control hardware outside the radio without resorting to the IEEE-488 interface.

The two front panel RF input relays, the RF input attenuator, and possibly a future ground loop isolator (GLI), are all controlled by a latch (U24) connected to the interface PCB data bus, through a relay driver (U1) which provides a 24 Volt source for each line. Separate connectors are provided for the input relay (J3), the RF input attenuator (J1), the GLI (J2), and the band select relay (J4). The relay driver and the connectors are provided with a separate ground return, kept independent all the way back to the power supply, for noise isolation. The relays are latching types, so the firmware will only drive them for a short time. The attenuator and GLI are non-latching, and will be driven continuously.

All latches coming off of the data bus are are cleared when the clear line from the processor PCB is strobed. This clear strobe is also passed on to the front panel displays and to the cardcage.

The interface PCB provides the source for the audible indicator function. This function has two destinations: the audible indicator on the switch/display PCB (a piezo transducer) and a mix into the audio output. Both begin the same way but end up being processed differently.

Two indications are possible, a short one and a long one. The duration of each is controlled by a one-shot pulse generator (U23), each triggered by a write strobe at a different address. The outputs of the two one-shots are ORed together (U25) to form an enable for the circuitry which follows. For the front panel transducer the enable signal is buffered by a gate (U25 again) and then drives a transistor switch on the switch/display PCB, which in turn sinks current through the transducer. Meanwhile, the enable also drives a transistor switch (Q2) on the interface PCB, which in turn switches a sine wave oscillator (U48, CR1, CR2, C67, C71, R3 - R6) on and off. The sine wave isn't very clean, but its fundamental is about 1 kHz, at about 1.5 Volts peak-to-peak. The output of the oscillator feeds one reference input of a dual 8-bit multiplying DAC (U49), which sets the amplitude of the signal from zero to full scale, in proportion to the code written into the DAC, from 0 to about 2 Volts peak-to-peak. The output of the DAC is current mode, and is converted back to voltage mode by and op-amp (U48 again). This signal is delivered to the X axis/audio amplifier PCB (A2A4) via a coax connector (J8). The other half of the dual DAC is used to set the amplitude of the front panel transducer. A -10 Volt reference (U51) supplies the reference, while another op-amp (U48 again) converts back to a voltage output. A transistor (Q1) is placed in the feedback loop to provide an adequate supply current for the transducer. The amplitude is again set in proportion to the code written into the DAC (a separate code, at a separate address, from that used for the audio amplitude), from 0 to +10 Volts.

The X axis output signal is also created here. The same -10 Volt reference (U51) feeds the reference of a 12 bit DAC (U50). The output of the DAC is converted to voltage mode by an op-amp (U48 again) and is passed to the X axis/audio amplifier PCB through a coax connector (J7). The signal amplitude is set in proportion to the code written into the DAC, from 0 to +10 Volts. In this case the code must be written in two pieces, first the upper four bits to one address, followed by the lower 8 bits to another. The data from the first write are not applied until the lower bits are written, at which time all twelve are applied simultaneously.

The interface to the processor PCB consists of address decoding to form chip selects and read and write strobes (U2 - U5, U25). Of the 256 addresses available from the 8 address lines, the mapping is implemented as follows:

Address 00(hex) - 7F(hex) = sent to cardcage

Address 80(hex) - AF(hex) = reserved by processor PCB

Address B0(hex) - FF(hex) = used by interface PCB

A detailed map of the R-110's bus addressing is given in Appendix B.

The physical interface to the switch/display PCB consists of two headers (J5, J6). The interface PCB mates directly to the back of it. The physical interface to the processor PCB consists of two more headers (P1, P2). The processor PCB mates directly to the back of the interface PCB.

4.8.3 X Axis Output Buffer

The X axis output from the interface PCB (A2A2) is buffered on the X axis/audio amplifier PCB (A2A4) on its way to the X axis output connector on the front panel. The buffer circuit consists of a one-pole R-C lowpass filter (R8, C18) and an input loading resistor (RX), followed by a unity-gain video buffer (U3). The filter has a corner at about 1.6 kHz and the buffer can drive the 0 to +10 Volt output of the X axis source into 50 Ohms if necessary. The circuit shares the PCB with the audio amplifier circuit. See paragraph 4.5.1 for a description of the power supply connections to this PCB.

4.8.4 Processor PCB (A2A3)

The processor PCB (A1A3) contains an 80C31 microcontroller, static RAM, EPROM, EEPROM, IEEE-488 and RS-232C interfaces, and several peripheral functions. The PCB manages all receiver operations and supports an interface bus for front panel and cardcage sensing, display and control. Figure 4-14 is a block diagram of the processor PCB.

The microprocessor (U7) operates on four address spaces, of which two are internal to itself and two are external. There are about 90 byte-wide internal RAM locations, some of which are addressed as special-purpose registers and some as general-purpose registers. Access to these constitues the first address space. Some of the registers may also be addressed as individual bits. 256 different internal bits may be accessed. This constitutes the second address space. Externally, separate address spaces are provided for instructions and data, with 65536 byte addresses available for each. Data addresses are read/write, while instruction addresses are read only.

The microprocessor currently operates with an 11.0592 MHz clock, based on a crystal (Y1). This clock rate provides a basic instruction cycle of 1.1 microseconds. The external data bus consists of eight address/data lines, eight upper address lines, read and write strobes for the data space, a read strobe for the instruction space, and a strobe for the required external lower address latch (U8).

Reset for the PCB is provided by a reset controller IC (U13). This resets the microprocessor directly on powerup and whenever the +5 Volt supply drops below 4.5 Volts. The microprocessor provides a number of discrete I/O pins, one of which is assigned as a soft reset. It is ORed with the output of the reset controller (U21). The combined reset is routed to the IEEE-488 controller on the processor PCB, and also strobes the clear line on the bus to the interface PCB (A2A2), which sends it in turn to the front panel displays and the cardcage. The reset controller is also connected to a pushbutton switch (S1) which provides a manual reset capability.

The microprocessor contains a serial port function. This becomes an RS-232 interface with the addition of a driver/receiver (U10) and a baud rate generator. One of the microprocessor's internal counter-timers provides the baud rate, using the processor clock as a reference. Discrete microprocessor I/O pins are used for DTR and RTS sensing, and DCD and DSR drive. A standard female DB-25 connector (J4) is provided on the PCB, but in normal use this connector is unavailable to the outside world. It is currently used for service functions only. It is configured as data communications equipment (DCE) so that it may be easily connected to the serial port of a computer.

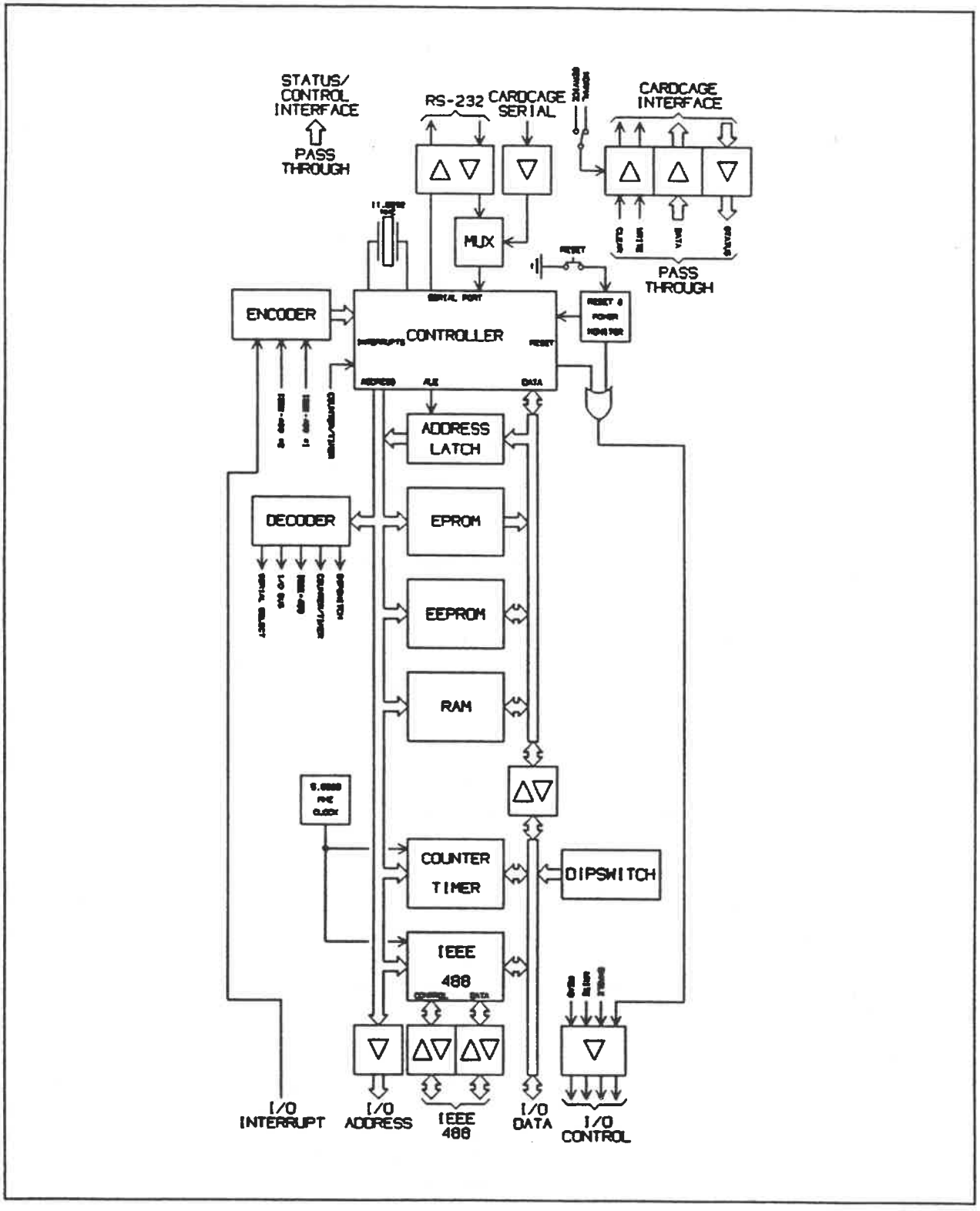

Figure 4-14: Processor PCB Block Diagram

The receive data line of the serial port is provided with a series of gates (U21, U23, U26) which select between the RS-232 driver receiver and a coax connector (J2), passed through a buffer (U6). This is currently unused, but is provided for a future application in which a plug-in module in the cardcage will need to return serial data to the microprocessor. Selection is controlled by a one-bit latch (U22) connected to the data bus.

The microprocessor contains two counter-timers. One is dedicated as the baud rate timebase for the serial port, as mentioned above. The other is used as a time clock, referenced to the microprocessor clock. It produces an internal interrupt about every 80 mS. The interrupt is used to do things (other than scanning) for certain fixed amounts of time, such as strobe the RF input select relay, which is a latching type and doesn't need to be continuously driven.

An external counter-timer IC (U19) is also provided. It is referenced to a separate clock oscillator (U24) running at 5 MHz. Although it contains three separate counter-timer circuits, the IC is dedicated exclusively to scan timing. All three circuits are connected in cascade, with the last output setting a status flip-flop (U22) which sends an interrupt request to the microprocessor. The microprocessor responds by stepping the scan and strobing a write address to clear the flip-flop. This address is shared with the serial port data select flip-flop, so while data isn't important when writing to clear the interrupt request, data must still be written so as to keep the serial select in the proper state.

The microprocessor provides two external interrupt request lines. One is dedicated to the external counter-timer. The other is driven by a priority encoder (U20) which presents an interrupt request and a two-bit code to the microprocessor. Three request lines drive the encoder, two from the IEEE-488 controller and one from the interface PCB. None are currently used.

The IEEE-488 controller (U27) is a TMS9914A, a standard implementation. It uses the 5 MHz oscillator as an operating clock, and standard driver/receivers (U28, U29) to connect it to the external bus. It may be configured as a talker or listener (in remote mode) or as a controller (in MDC mode). The device trigger function, DMA, and service request interrupts are currently unused.

An eight-bit dipswitch (S3) is routed to the interface bus through a tristate buffer (U17). It is currently used to set the IEEE-488 interface address for the radio (factory setting is 16) and the serial port baud rate (factory setting is 1200).

External permanent memory is provided by a 32k x 8 EPROM (U11). This contains the operating instructions for the microprocessor and most of the fixed data tables. It is located in the lower half of the instruction address space. The lower half of the data address space, minus the last 256 bytes, is occupied by a 32k x 8 EEPROM (U14), which, while permanent, may be reprogrammed repeatedly in socket. It contains changeable data tables and provides the nonvolatile storage capability. The upper halves of both memory spaces are combined and shared by a 32k x 8 RAM (U12). This provides volatile data storage, and also, since it is shared between the memory spaces, allows code to be loaded on the fly and then run, as an aid to development, initialization, and service. The remaining 256 bytes of the data space is reserved for I/O functions, for which an interface bus is provided.

Provision is made for future expansion of the operating code. When the code exceeds 32k bytes a larger EPROM will be required. When this happens a 64k part will be adopted. Jumpers (E1 - E9) are provided to accommodate this. It will cause the address map to change, because the upper halves of code and data memory can no longer be shared. It will no longer be possible to download code and execute it on the fly.

The main address decoder consists of gates (U9, U23, U26) which divide the external memory spaces in half and then identifies the last 256 bytes of the first half of the data space for I/O. This circuit is also used to subtract this segment from the memory space of the EEPROM (U14), which would otherwise also be selected.

Secondary address decoding is provided for the peripheral functions. A decoder (U18, U21) maps the on-board peripherals into the I/O space. A detailed hardware memory map is provided in Appendix B, but here is the map for the processor PCB, in short form:

Code Address 0000(hex) - 7FFF(hex) = EPROM (U11)
Code Address 8000(hex) - FFFF(hex) = RAM (U12) (shared)

Data Address 0000(hex) - 7EFF(hex) = EEPROM (U14)
Data Address 7F00(hex) - 7FFF(hex) = I/O (see below)
Data Address 8000(hex) - FFFF(hex) = RAM (U12) (shared)

I/O Address 80(hex) - 83(hex) = dipswitch (S3, U17) (read)
I/O Address 80(hex) - 83(hex) = external counter-timer interrupt clear (U22) (write)
I/O Address 80(hex) - 83(hex) = serial receive data select (U22) (write)
I/O Address 84(hex) - 87(hex) = external counter-timer (U19)
I/O Address 88(hex) - 8F(hex) = IEEE-488 controller (U27)

The dipswitch, external counter-timer interrupt clear, and serial port receive data select are all redundantly mapped -- that is, only one address is required to perform the functions, but they are mapped to four addresses for ease of address decoding. I/O addresses which are not used by the processor PCB -- 00(hex) - 7F(hex) and 90(hex) - FF(hex) -- are available for use by the interface PCB, the front panel displays, and the cardcage.

The I/O bus is taken from the microprocessor bus by passing the data lines through a tristate transceiver (U16), the first eight address lines and the read and write strobes through tristate buffers (U15, U25), and the combined clear line and a bus enable line (developed by the address decoding circuit) through more buffers (U25). The bus enable line also enables the transceiver and tristate buffers, so that the I/O bus is at high impedance (and pulled up) when not in use. This bus is routed to the interface PCB, which in turn routes it to the front panel displays. The link to the cardcage begins at the interface PCB, but must pass back through the processor PCB to get there. This link is completely independent of the other circuitry on the processor PCB, even to the extent of having its own separate power supply and ground return. Buffers (U1 - U3) are hooked to this clean power to act as a data line filter between the control section and the cardcage. Status return lines from the cardcage and the power supply are also buffered (U4 - U6) to provide filtering. These buffers are normally always enabled, but a switch (S2) is provided which will tristate them when they are not actively in use, as a service aid.

The lines running from the interface PCB to the rear panel status/control output connector also pass through the processor PCB, but there is no circuitry involved other than traces to link the input and output connectors.

4.8.5 IEEE-488 Interface

Following is a general description of the IEEE-488 interface. Descriptions of bus commands are given in Appendix A.

The IEEE-488 interface is a digital data communications interface consisting of eight parallel data lines, eight control lines, and eight ground lines. A double-row 24 pin connector is specified for the interface, along with jackscrew retainers. The complete specification is given by the Institute of Electrical and Electronics Engineers (IEEE) as their specification number 488, copies of which are available from them. There are now two parts to the standard, 488.1 and 488.2. The first part is mostly a hardware and timing specification, while the second part defines various command, query, and response protocols.

The specification defines three sorts of devices which may be connected to the bus. These are controllers, talkers, and listeners, and a particular piece of hardware may be any or all of these. There may be multiple controllers on the bus, but only one may be active at any given time. A protocol is defined whereby active control may be passed from one to another. One of the controllers is considered to be "system controller", meaning that it may regain control of the bus whenever it wants to without resorting to the normal transfer protocol.

The controller assigns other devices on the bus as active talkers or listeners. There may be only one active talker at a time, whereas there may be multiple listeners. The active talker drives the eight bus data lines, and the listeners sense them. The controller may make itself a talker or listener as well.

Three of the control lines act as handshaking for transfers on the data lines. The active talker drives **Data Available** (DAV) and the listeners share control of **Not Ready for Data** (NRFD) and **Not Data Accepted** (NDAC). Each byte transferred across the data lines goes through a handshaking protocol in which the talker signals that data is available and all listeners must acknowledge when they receive it. The speed of the transfer is therefore determined by the response time of the last listener to acknowledge.

There remain five other control lines. These are described as follows:

Attention (ATN): The ATN line is used by the controller to interrupt the currently active talker. When ATN is asserted the talker stops driving the data and DAV lines and everybody waits for the controller to send a command. With ATN asserted the controller can then drive the data and DAV lines and issue commands. Commands are received by all devices on the bus, regardless of their currently assigned state. When the controller stops asserting ATN it also stops driving the data and DAV lines, and any assigned talker can then resume driving them.

Remote Enable (REN): The REN line is driven by the controller in charge and allows devices on the bus to be placed under control of the bus when it is asserted. When the controller stops asserting it, all devices on the bus return to local (manual) control.

Interface Clear (IFC): The IFC line is strobed by the controller in charge when it wants to reset the system to its base state. It acts as a master reset.

End or Identify (EOI): The EOI line is unique in that it is the only line with more than one function. In conjunction with a command state (ATN asserted) it triggers parallel polling. In conjunction with a data state (ATN unasserted) it can be used to indicate the last character of a data string.

Service Request (SRQ): The SRQ line is the only control line other than handshaking that is driven by the bus slave devices rather than the controller. The line is used as an interrupt request and is shared by all devices on the bus not in control. When the controller senses it being asserted it must serially poll the devices on the bus which may be responsible for asserting it. Several devices may assert it simultaneously.

4.8.6 Microprocessor Firmware

The firmware that controls the 80C31 microcontroller consists of two major sections: the monitor and the application code. The monitor acts as a mini-operating system which can converse with an operator over the RS-232 interface and also run the application package. It is resident at the bottom of code memory, so that it contains the first level of interrupt and reset servicing as well. The RS-232 capability is limited to service functions at the present time: if no video terminal is connected, then execution automatically branches to the application code from the monitor on powerup (after some initialization of hardware and storage).

The application code senses the settings of the front panel controls (in local modes), the status from the various sections, and the status of the IEEE-488 and RS-232 interfaces. Based upon these inputs, it determines the operating modes of the receiver and what action needs to be taken. It sends data to the front panel indicators and displays, to the receiver hardware, and to the IEEE-488 interface.

The monitor is structured as a loop which waits for input from the RS-232 interface. When it receives data, it parses it against its list of legal command forms. If no match is found, then it will send an error message and resume the input loop. If the command is successfully parsed, then the monitor will execute the command and then, unless the command causes execution to branch out of the monitor, it will again resume the input loop.

The 80C31 microcontroller delegates specific addresses at the bottom of code memory for reset and interrupt branch locations. These branches are handled automatically by the microprocessor without recourse to the firmware, but firmware must be present at these locations to control the servicing of these functions. Resets are serviced by branching to the monitor startup code, which initializes the microprocessor hardware. Interrupts are handled by branches to specific locations in the application code.

The application code begins by initializing its storage, the front panel hardware state, and the RF section hardware state. It then begins a polling loop which checks various front panel controls, IEEE-488 interface status, RF, IF, video and synthesizer section status, and power supply status. New control values read from the front panel, etc., are compared against stored previous values. Any difference causes a dedicated subroutine to be executed to service the change. Interrupts are briefly enabled in the polling loop between one individual status check and the next. This prevents interrupts from occurring during servicing of differences, since this servicing often uses subroutines and storage that is also used by the interrupt service routines, and these routines are neither recursive nor re-entrant.

Meanwhile, a timeclock (based on an internal timer in the 80C31 and referenced to the microprocessor clock) is continuously running. It requests an interrupt every 80 msec or so, and is used for functions that require real-time delays (scanning excepted). The service routine checks to see what is enabled and which of those need servicing. It calls a separate service routine for each one that needs it. A separate hardware timer is used for scanning. It is programmable to four or more digits of resolution, and is used to request interrupts for updates of the cardcage hardware and the front panel during scans, at the specified step rate.

The application code uses all five of the available memory addressing modes: internal bit, internal byte, internal stack, external code, and external data. Internal bit addresses not dedicated to hardware registers are used for application code flags. Remaining internal RAM is divided between stack space and most-often-used or time-critical single-byte storage. External instruction memory in part holds the application and monitor code (EPROM), and also tables of fixed data. External data memory holds the I/O map, nonvolatile read/write storage (EEPROM), and volatile read/write storage (RAM). The I/O map provides a firmware connection to hardware other than RAM, EPROM and EEPROM located outside of the 80C31. Nonvolatile read/write storage holds the calibration tables and data, and nonvolatile state storage. Volatile memory holds the working data and storage that can't fit into the internal RAM of the microprocessor, and also the volatile state storage. In addition, since upper external instruction and data space is shared, code can be loaded into RAM and run as well.

The firmware is written in assembly language for the 80C31 microcontroller, using a number of macros to effectively extend the instruction set. While the assembler and linker allow for relocation of modules, at the present time all object code is ORGed to absolute addresses.

4.9 Power Supply

The power supply section has been designed to provide regulated DC power for the receiver electronics while minimizing conducted and radiated interference. The supply uses extensive shielding and filtering, toroidal magnetics, and special mechanical construction techniques to reduce emissions and to control susceptibility. Figure 4-15 is a block diagram of the power supply.

The power supply is part of the rear panel assembly of the receiver, and consists of a housing containing an input power receptacle, fuses, and EMI filters, a toroidal power transformer, line voltage selection switches, a cooling fan, and a PCB including rectifiers, filter capacitors, linear regulators mounted on heat-sink sub-assemblys, voltage monitors, and the DC output connector. The fuses interrupt the line power if the receiver is connected to an improper voltage or if internal malfunctions occur. Monitor circuits on the rectifier/regulator PCB check the line and the power supply outputs for out-of-tolerance conditions, driving indicators on the front panel and providing status signals for the IEEE-488 interface and the rear panel's status/control output connector.

Functionally, the power supply consists of three main parts: the unregulated supply, the regulated supply, and the voltage monitors. The DC voltages available from the regulated supply are shown in table 4-11.

Table 4-11: Power Supply Output Connector Pinout

Output Name	Power Supply Connector Pin	Destination(s)
+5 VDC	15	Cardcage, Front Panel Buffer
+5 RTN	16	Cardcage, Front Panel Buffer
Front Panel +5 VDC	1	Front Panel Logic
Front Panel +5 RTN	3	Front Panel Logic
Switch +5 VDC	14	Front Panel Pushbuttons
Switch +5 RTN	16	Front Panel Pushbuttons
+8 VDC	12	Cardcage
+/-8 RTN	25	Cardcage
-8 VDC	13	Cardcage
+15 VDC	11	Cardcage, Front Panel Audio
+/-15 RTN	23	Cardcage, Front Panel Audio
-15 VDC	24	Cardcage, Front Panel Audio
Front Panel +15 VDC	9	Front Panel Logic
Front Panel +/-15 RTN	7	Front Panel Logic
Front Panel -15 VDC	21	Front Panel Logic
Audio Output +15 VDC	10	Front Panel Audio
Audio Output +/-15 RTN	19	Front Panel Audio
Audio Output -15 VDC	22	Front Panel Audio
+24 VDC	6	Front Panel Logic
+24 RTN	8	Front Panel Logic
+50 VDC	18	Cardcage
+50 RTN	20	Cardcage
AC High Status	5	Front Panel Logic
AC Low Status	17	Front Panel Logic
DC Unreg Status	4	Front Panel Logic

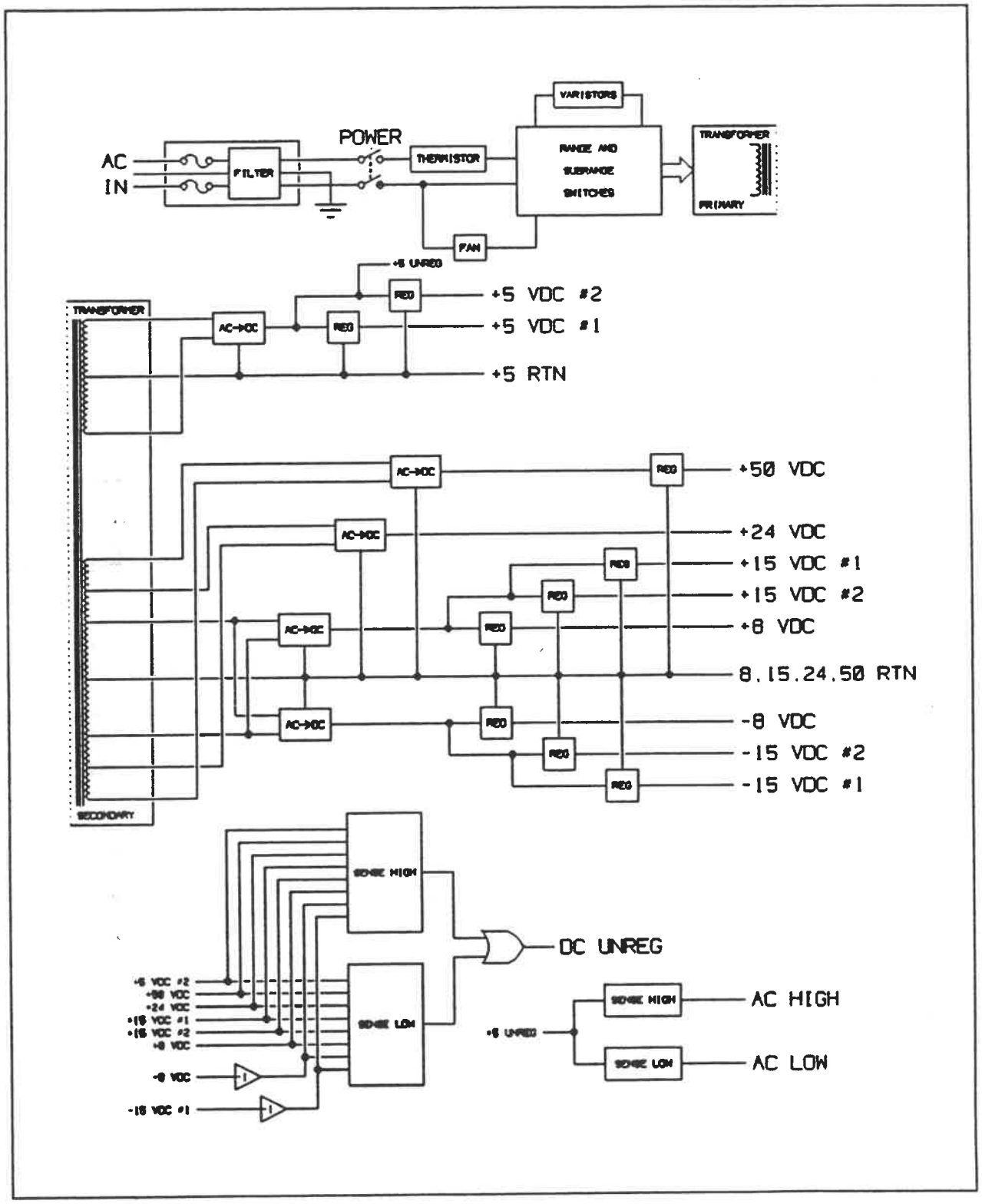

Figure 4-15: Power Supply Block Diagram

4.9.1 Unregulated Supply

The unregulated supply consists of the AC receptacle with fuses and EMI filtering, the inrush limiter, the front panel power switch, the fan, the AC voltage range switches, the line spike suppressors, the power transformer, the rectifiers, and the filter capacitors. Power enters the unit via the line receptacle, which contains the line filters and a pair of fuse holders. One is used for line and one for neutral when connected to 115 VAC; for 230 VAC, one is used for each of the hot lines. The line filter is designed to provide 30 - 50 dB of bidirectional filtering of frequencies in the kHz-MHz range. After passing through the fuses and EMI filter, the AC is routed to the front panel power switch. For 115 VAC operation, both hot and neutral are switched; for 230 VAC, both hot lines are switched. AC from the power switch returns to the rear panel, passes through a thermistor (TM1) to reduce the surge at powerup, and is bypassed with a pair of varistors (VR1, VR2). These devices shunt very short duration spikes, providing line spike protection for the receiver.

The AC then goes to the voltage selection switches. The AC voltage range switch selects either 115 or 230 volt operation by connecting the dual primaries of the power transformer (T1) in parallel or in series, respectively. The AC voltage subrange switch selects one of six line conditions, from well below nominal to well above, by selecting one of six taps on one of the power transformer primaries for service. The fan is connected across the transformer primaries so it always receives 115 VAC no matter whether 115 or 230 VAC is applied to the receiver.

The power transformer has eight secondary windings. Two are used as a center-tapped source for the rectifiers (D10, D11) supplying the +5 VDC regulators. The other six windings are "stacked" to yield a multiple-tapped secondary feeding the rectifiers for the +50 (D2, D3), +24 (D4, D5), and +/-15 VDC (D6 - D9) outputs. The +/-8 VDC outputs are derived from the same rectifiers that feed the +/-15 VDC outputs.

Rectifying and filtering circuits are mounted on the printed circuit board. Discrete rectifiers are connected for full-wave rectification in all circuits. The transformer windings, harness, and circuitry are specially configured to reduce noise caused by high crest-factor currents: each winding on the transformer terminates at the same point (no hybrid connections within the transformer), twisted pairs attach to the terminations, harness geometry is controlled, rectifiers are located close to their power source, diode packs are used to reduce wire length, etc.

4.9.2 Regulated Supply

The regulated portion of the power supply consists of part of the printed circuit board, plus the heat sink assemblies mounted to it. Overall, the PCB contains the rectifiers and filter capacitors of the unregulated supply, regulator components, the AC line-range detectors, and the regulator status monitor.

All regulators except for +24 VDC and +50 VDC are implemented with low-dropout linear integrated circuit devices which operate with minimal headroom; these improve the efficiency of the power supply, cutting both power consumption and power dissipation. The +50 VDC regulator uses a linear integrated circuit regulator as well, but with normal headroom constraints. However, current draw on this output is minimal. Each regulator incorporates short circuit protection and thermal overload protection. The +24 VDC supply is unregulated, but is used only to drive relay coils, an application for which regulation requirements are minimal. Protection is nevertheless provided by a series resistor which will limit the current drawn in case of a short circuit.

All DC outputs except for +24 VDC are fixed in amplitude using precision resistive dividers or fixed-value ICs. No trimming of the output voltages is available.

4.9.3 Power Supply Monitoring

The power supply monitor circuits check for AC line high and low, and regulated output high and low for most of the DC outputs. Most of the checking is done with a pair of power supply monitor ICs (U10, U11). These ICs use timing capacitors (C26 - C31) to allow the ICs to ignore short glitches in the output. A reference is provided in each IC, set to 2.5 VDC. This establishes the undervoltage comparison thresholds for both the regulator and line monitors. An external resistive divider (R32, R36) divides the reference to 1.7 Volts to provide the regulator overvoltage comparison threshold. The voltage sense lines pass through resistive dividers to properly match these thresholds. Monitor functions are as follows.

For line voltage high detection, unregulated +5 VDC is divided (R22, R35) and compared to the reference by the line low sense circuit of one of the monitor ICs (U11). In normal operation the sensed voltage is lower than the reference and therefore a fault status is generated. This status is inverted by a transistor switch (Q1) so that status is now good when the sensed voltage is below the reference. The output of the transistor forms the AC line high status signal and is sent to the front panel logic circuitry for processing and distribution.

For line voltage low detection, unregulated +5 VDC is divided (R20, R33) and compared to a reference by the line low sense circuit of the other monitor IC (U10). In normal operation the sensed voltage is above the reference and therefore no fault condition is generated. The output from the monitor IC forms the AC line low status signal and is sent to the front panel logic circuitry for processing and distribution.

For DC regulation monitoring, both overvoltage and undervoltage conditions are sensed, based on comparison to a reference and a fixed fraction of it. Note that sensing is reversed from what is normally expected, because the undervoltage threshold is higher (2.5 Volts) than the overvoltage threshold (1.7 Volts). What happens is that the monitor internally adds the reference to a quarter of the external threshold comparison voltage, producing an internal overvoltage comparison threshold of 2.925 Volts. Each monitor IC produces both undervoltage and overvoltage status signals; all four signals are combined using open-collector drivers (U12) to form a single regulation status line which is sent to the front panel logic circuitry for processing and distribution.

One IC (U10) monitors the cardcage +/-15 VDC and +/-8 VDC lines, while other (U11) monitors +24 VDC, +50 VDC, cardcage +5 VDC, and front panel +15 VDC (shared by front panel logic and the audio output). This leaves front panel +5 VDC and front panel -15 VDC unmonitored, but the front panel +5 VDC may be omitted because without it the front panel logic will not be able to receive and process the status information anyway. Note that a resistor (R38) is used to further loosen the tolerance on the +24 VDC monitor line.

4.9.4 Power Supply Usage

The power supplies are used by the various modules and assemblies of the radio as shown in table 4-12.

Table 4-12: Power Supply Usage

	+5 #1	+5 #2	+8	-8	+15 #1	-15 #1	+15 #2	-15 #2	+24	+50
Control Section	X	X					X	X	X	
X Axis/Audio Amplifier PCB					X	X	X	X		
Microwave RF Module		X		X	X					
Preselector Module		X			X	X				
Low Frequency RF Module			X	X	X					
21.4 MHz IF Amplifier Module		X	X	X	X	X				
21.4 MHz IF Filter Module			X	X						
Video Module		X	X	X	X	X				
DCIF Module		X	X	X	X	X				
Fixed LO Synthesizer Module		X			X	X				
Low Frequency Synthesizer Module		X			X	X				
Microwave Synthesizer Module		X			X	X				X

4.10 Chassis Wiring

There is very little discrete chassis wiring in the R-110. The most obvious wiring is the coax harness running across the tops of the cardcage plug-in modules. These are shown in the harness diagram (493055) provided in section 6. An additional coax harness (493750, 493755) is provided in the rear panel assembly to connect the rear panel monitor jacks. See the assembly drawing (493700) for placement. The front panel assembly also contains coax cables, both flexible and semi-rigid (493670, 493671). See the assembly drawings (493600, 493607) for placement. Several front panel subassemblies sport pigtails which plug into printed circuit boards. Wiring of a given pigtail is part of the associated subassembly. See the front panel assembly drawings and the schematic (493601) for details.

Three ribbon cables are required. One 37 conductor ribbon links the front panel assembly to the cardcage backplane. A shielded 24 conductor ribbon extends the IEEE-488 interface from the front panel assembly to the rear panel connector. A shielded 25 conductor ribbon links the rear panel status/control output connector to the front panel assembly. All of these are captive to the cardcage assembly. See the assembly drawing (493050) for details.

An eight-wire pigtail (493065) links the microwave RF module (A1A1) to the cardcage backplane. This pigtail plugs in at each end, and is not captive to the cardcage.

The rear panel assembly contains discrete wiring for the AC input module, the range switch, and the fan. A four-wire pigtail is provided for connection of the power switch on the front panel, and a two-wire pigtail is provided for connection of the fan. All DC power comes from a 25 pin D-sub connector on the power supply printed circuit board. See the assembly drawing and schematic (493700, 493701) for details.

Finally, the cardcage is provided with a wiring harness. One part of this harness is a four-wire pigtail which links the front panel power switch to the rear panel assembly. It mates with connectors at both the front and rear panels. The rest of the harness provides DC power distribution for the front panel and the cardcage. A 25 pin D-sub connector brings power from the rear panel assembly, and delivers it to the front panel assembly via 9 pin and 15 pin D-subs. The harness is captive to the cardcage, and is hard-wired to it via feed-through capacitors. Power wiring passes through the feed-throughs and ends at soldered connections to the cardcage backplane. See the assembly drawing and schematic (493050, 493051) for details.

Discrete wiring in the R-110 is color coded, where possible. DC power supply voltages and returns are each given a unique color code. Signal wiring is more limited. See table 4-13.

Table 4-13: Discrete Wire Color Coding

Usage	Color
+5 VDC	Green
+5 RTN	White/Green
+8 VDC	Brown
8 RTN	White/Brown or White/Blue
-8 VDC	Blue
+15 VDC	Red
15 RTN	Gray
-15 VDC	Violet
+24 VDC	Orange
+24 RTN	White/Orange
+50 VDC	Yellow
+50 RTN	White/Yellow
AC (Line)	Black and White Twisted Pair
Signals	White or White/Black
Signal Ground or Non-Specific Ground	Black
Coax	Unspecified